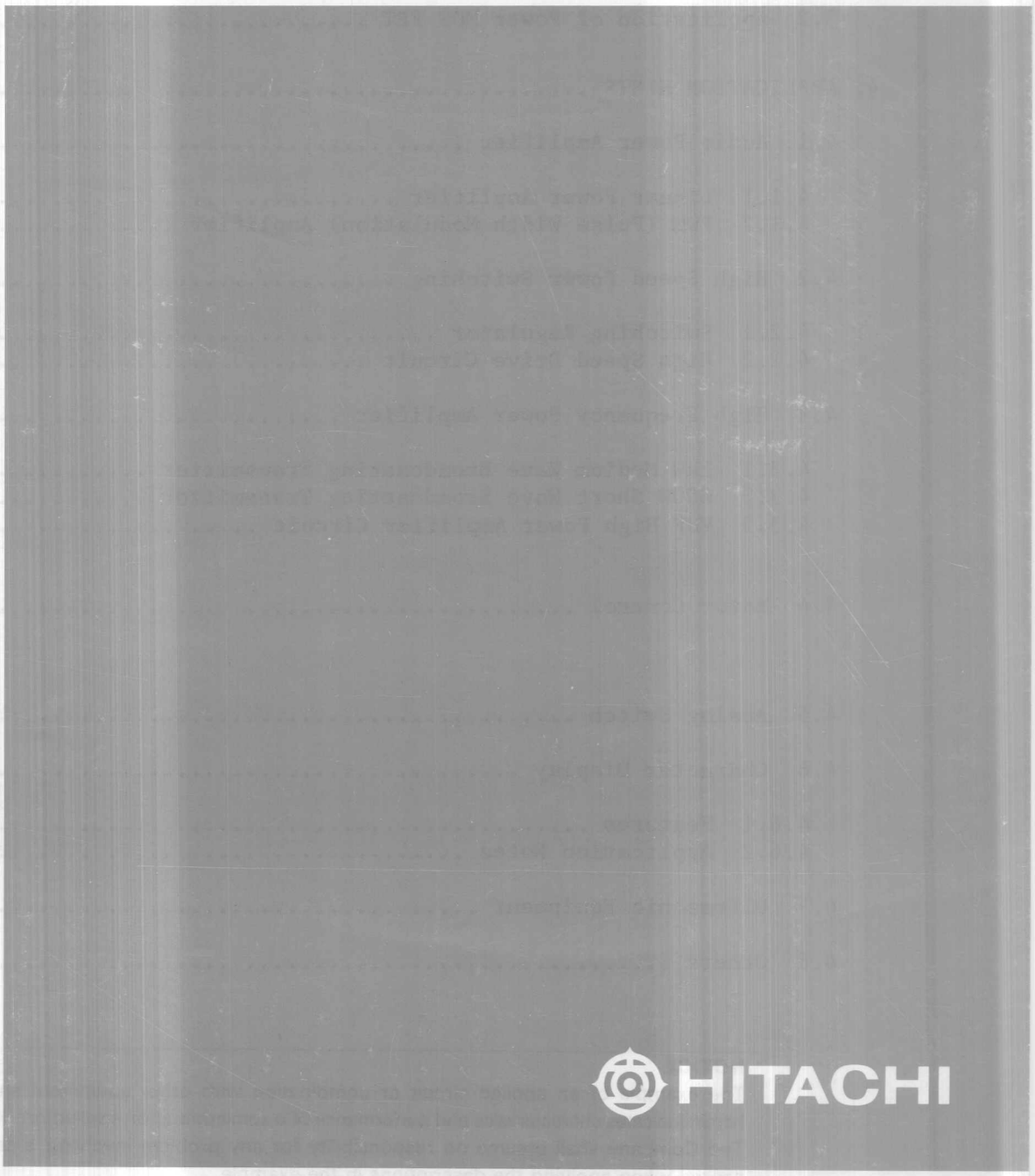
APPLICATION NOTE

Power MOS FET



HITACHI

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HITACHI

1. INTRODUCTION

In 1977, HITACHI was the first in the world to develop and mass-produce 100 Watt Complementary Power MOS FETs. Since then, Power MOS FETs have been used in a variety of fields as an ideal power device with high switching speed and high resistance to electrically induced failure. HITACHI Power MOS FET technology has consistently advanced in the areas of on-resistance, voltage and current handling capability and packaging.

POWER MOS FET FEATURES:

A. Excellent frequency response and high switching speed. (No carrier storage effects.)

B. High resistance to electrical destruction. (No current concentration effects.)

C. Easy parallel connection for higher power applications.

D. Minimum drive power. (Voltage controlled device.)

There are two basic Power MOS FET structures: Vertical Type and Lateral Type. The advantages of Vertical Types are: a) Drain Case and b) low on-resistance and low loss. Advantages of Lateral Types are: a) Source Case, b) high resistance to electrical destruction, and c) high frequency response. HITACHI has both types to meet various requirements. The Vertical Types are called "D Series", and the Lateral Types are called "S Series".

Power MOS FETs show extreme advantages, not only in new fields where conventional power devices are inadequate, but also in existing fields where conventional devices are already in use.

2.STRUCTURE & FEATURES

Hitachi has two types of Power MOS FETs, D Series (vertical structure) and S Series (lateral structure), as shown in Fig. 2-1 and Fig. 2-2. Although there are some differences in their characteristics, both have the following advantages.

- Good frequency response and high switching speed due to absence of carrier storage effect.
- Free from current concentration, and hence have high resistance to destruction.
- Require a very low driving power as they are voltage controlled devices.

To understand the structure and features of Power MOS FETs, we would like to show the N-channel MOS FET.

Fig. 2-3 shows the N-channel MOS FET structure. This is called an MOS structure, because the current control gate region is made of three layer, Metal, Oxide and Silicon. The charged particles (electrons, here) are produced from Source and flow to and out of Drain.

When a positive voltage is applied to the gate electrode, in proportion to it, a depletion layer will be produced on the silicon surface beneath the gate. Then negative charges (electrons) will appear on it, which cause the silicon surface to be inverted from P type substrate to N type layer. This inverted layer is channel..

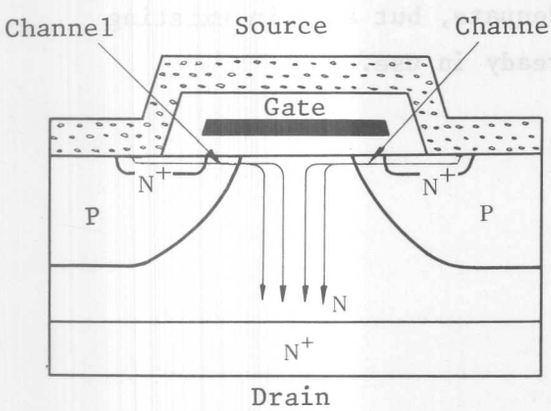


Fig. 2-1 Structure of D series (Vertical type) (N channel)

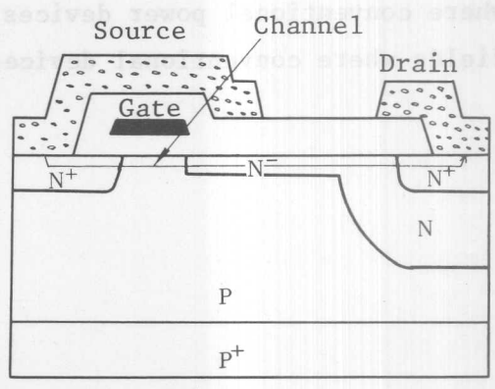


Fig. 2-2 Structure of S series (Lateral type) (N channel)

When a voltage is applied between Drain and Source, electrons in the channel will move to the Drain, which means that the drain current flows.

There are two types of FETs, depletion type (normally ON type) and enhancement type (normally OFF type). In the case of depletion type FETs, drain current flows even if the gate voltage is OV, in contrast to enhancement type FETs. Hitachi Power MOS FETs are all enhancement type (normally OFF type).

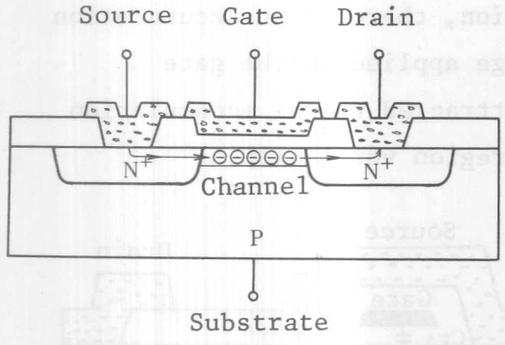


Fig. 2-3 Basic Structure of MOS FET (N channel)

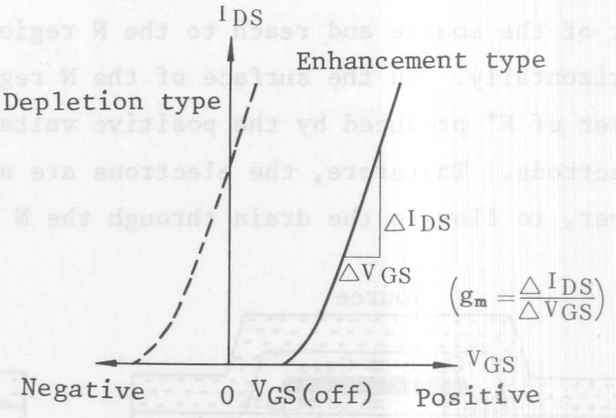


Fig. 2-4 Transfer Characteristics

The gate voltage at which the drain current begins to flow is gate cut-off voltage $V_{GS}(off)$. (Fig. 2-4).

Normally, there is a quadratic correlation between I_{DS} and V_{GS}. The slope of its curve gives the mutual conductance $g_m(=\frac{\Delta I_{DS}}{\Delta V_{GS}})$, that shows amplification factor.

Breakdown voltage of the drain varies with the structure between the N^+ region of the drain and the gate electrode, as shown in Fig. 2-3. There is only a thin oxide film between the N^+ region and the gate electrode, so the field gradient will be high. This makes it difficult to achieve high drain to gate breakdown voltage, limited to 20 ∿ 30V in typical MOS FETs.

By widening the space between the N^+ region of the drain and the gate electrode, and easing the electric field concentration, we can make the breakdown voltage larger.

There are two fabrication methods used to make the breakdown voltage higher, one is D series (vertical structure) and the other is S series (lateral structure). We would like to further explain about their structures and features, with Fig. 2-1 and Fig. 2-2.

● D Series (vertical structure)

In D series the drain (N^+) is placed beneath the silicon substrate. The gate electrode covers over the N region between P channels, to ease the electric field concentration beneath the gate. The electrons flow out of the source and reach to the N region through the P channels horizontally. On the surface of the N region, there is an accumulation layer of N^+ produced by the positive voltage applied to the gate electrode. Therefore, the electrons are attracted to the accumulation layer, to flow to the drain through the N region vertically.

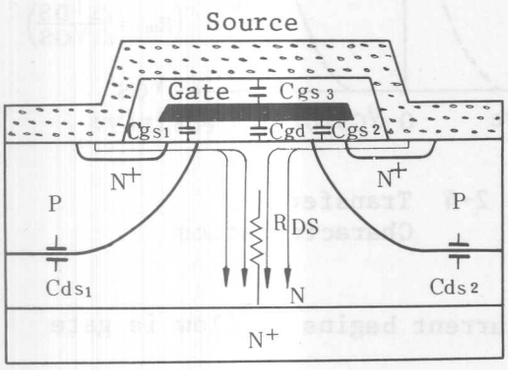


Fig. 2-5 Structure of D series (Vertical type) (N channel)

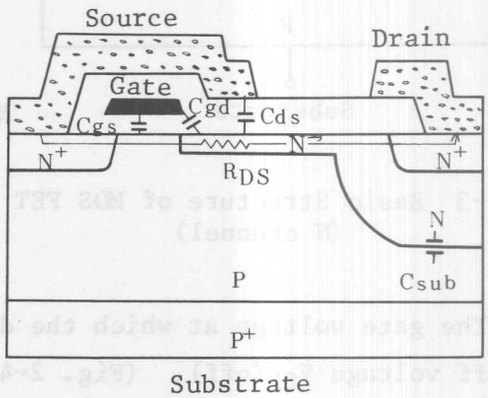


Fig. 2-6 Structure of S series (Lateral type) (N channel)

$C_{GS}=C_{gs1}+C_{gs2}+C_{gs3}$

$C_{DS}=C_{ds1}+C_{ds2}$

$C_{GD}=C_{gd}$

Consequently, the D series is referred to as a vertical structure. In this structure, the case is connected to the drain.

In the D series the channel (N region) is placed in the silicon, and the size of one unit can be smaller than that of S series. This enables the switching ON resistance of D series to be smaller than that of S series with the same voltage and the same chip size.

Electrostatic capacitances are the junction capacitances and the MOS capacitances as shown in Fig. 2-5.

Here, the capacitance between the drain and the gate, C_{GD}, is relatively large, so in the source earth circuit, C_{GD}'s effects to the input capacitance (Ciss), to the output capacitance (Coss) and to the feedback capacitance (Crss) should be considered.

The gate electrode is made of polysilicon, which has long been used effectively in CMOS LSI. Polysilicon resistance is about 100 times larger than that of metals such. When using it for the gate electrode, we lower the gate resistance by using a mesh gate pattern, and by connecting the polysilicon gate and the metal electrode effectively. To find the switching time of the vertical structure, more complicated operation analysis is required, because the feed back capacitance (Cgd) is large and the voltage dependence of the drain resistance is large. The input capacitance can't be determined simply by the time constant of the gate resistance. This will be further explained in the switching characteristics, paragraph 5.3.

● S Series (lateral structure)

In S series, the drain (N^+ region) is placed on the surface of the silicon. The region between the drain (N^+) and P channel is an N region produced by ion implantation, and it makes the strength of the electrostatic field even. Moreover, the source electrode is extended to cover a part of the N region, working as a field plate to prevent electrostatic field concentration around the gate. The electrons flow out of the source and reach to the drain through the P channel and the N region laterally. This is why the S series is called a lateral structure.

The substrate is connected to the source electrode, and the case to the source.

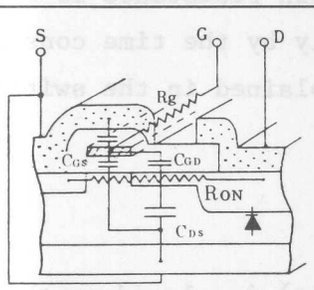
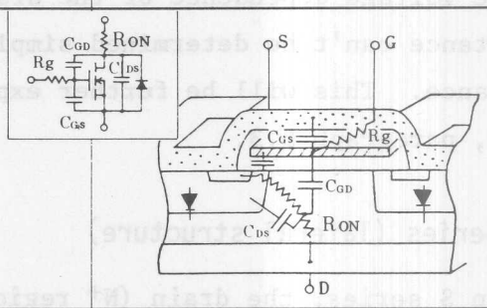
The feed back capacitance (Crss) is indicated as Cgd in Fig. 2-6. The source field plate is extended above the N region, so the Cgd is shielded by the field plate and the capacitance of the N region (Cds). This results in a very small value of feed back capacitance (Crss).

2.STRUCTURE & FEATURES

From the view points of chip and package, the S series is very suitable for high frequency use, because the input and the output leads are separated electrically. Like in the D series, we usually use polysilicon for the gate electrode. Moreover, we can provide devices with metal gates for very high speed. In the polysilicon gate FET, the frequency limit is determined by the time constant of the input capacitance and the gate resistance. In the metal gate FET, it is determined by the lead inductances of the gate and the source, because the gate resistance is very small.

Table 2-1 shows the small signal equivalent circuit and the typical characteristics of D series and S series.

Table 2-1 Equivalent Circuits and Features, Parameters

Item \ Structure		Off-set Gate Type	Vertical Type
Equivalent Circuit			
Features	R_g	Large (22Ω)*, However, it is able to be decreased by 2 figures with Metal-gate	Small (2.5Ω)*
	C_{iss}	Small (800pF)**	Large (1800pF)**, C_{GD} is increased enormously at low Drain Voltage
	C_{oss}	Large (350pF)**	Small (190pF)**
	C_{rss}	Small (15pF)**, Slightly depend on Drain Voltage	Large (85pF)**, C_{GD} heavily depends on Drain Voltage
	R_{ON}	Large(2.2Ω)*	Small (1Ω)*
	g_m	Small (1.0S)*	Large (1.8S)*
	ASO	Good	Fair

(Note) * Typical value of V_{DSS}=400V, I_D=5A rating.

** Test Condition : V_{DS} = 10V, V_{GS} = -5V, f = 1MHz

Table 3-1 D Series Line-up

V_{DS}(V) \ I_D(A)	0.3	1〔1.5〕	2	3	5	6	7	8	10	12	15	30〔25〕	50
40			□2SK416(0.5) □2SJ120(1.2)		▲2SK345(0.3) ▲2SJ102(0.3)								
60					▲2SK346(0.3) ▲2SJ102(0.3)				▲2SK428(0.1) ▲2SJ122(0.15) ▲2SK549(0.1)			▲2SK600 (0.04)	
80					▲2SK294(0.4)								
100				□2SK429(0.5)	▲2SK295(0.4)				▲2SK383(0.15) ○2SK398(0.2) ○2SJ112(0.25) ●2SK399(0.2) ●2SJ113(0.25)			○2SK561* (0.05)	
120									○2SK308(0.2) ▲2SK551(0.15)* ▲2SJ127(0.2)*				
140								●2SK413(0.4) ●2SJ118(0.4)					
150				□2SK430(0.8)									
160								●2SK414(0.4) ●2SJ119(0.4)					
200						▲2SK440(0.4)		●2SK400(0.5) ●2SJ114(0.6)					
250	■2SK511(30)								○2SK401(0.3) ●2SK412(0.3)				
300		▲2SK296(2.5) □2SK375(2.5)											
400		□〔2SK535〕(4.0)	▲2SJ117(5.0)	▲2SK310(2.5)	▲2SK319(1.1)			○2SK298(1.1) ○2SJ116(1.8) ●2SK402(1.1)	●2SK349(0.67)				
450		□〔2SK579〕(5.5)		▲2SK311(2.5)	▲2SK320(1.1) ▲2SK552(1.0)		▲2SK554(0.6)	○2SK299(1.1) ●2SK403(1.1)	●2SK350(0.67)	○2SK313(0.67) ●2SK556(0.35)	●2SK559(0.25)		◇PM4550C(0.13)
500	□2SK384(25)	□〔2SK580〕(6.0)	▲2SK382(2.5)		▲2SK553(1.2)		▲2SK555(0.7)			●2SK557(0.45) ○2SK512(0.55)	●2SK560(0.3)	◇HS7920(0.2)*	◇HS7910(0.12)*
800				▲2SK513(5.0) ●2SK415(5.0)	○2SK351(1.7) ●2SK534(3.0)								

Note 1.
* : Under Development
( ) : $R_{DS(on)}$ typ

Note 2. Package
□ : DPAK
■ : TO-126
△ : TO-39
▲ : TO-220AB
○ : TO-3
● : TO-3P
▽ : RFPAK
◇ : Module

Table 3-2 S Series Line up

I_D(A) / V_{DS}(V)	0.5	1.5	2	4	5	7	8
120						○2SK133(1.0) ○2SJ48(1.0)	
140	▲2SK213(8) ▲2SJ76(10)					○2SK134(1.0) ○2SJ49(1.0)	
160	▲2SK214(8) ▲2SK214Ⓚ(8) ▲2SJ77(10) ▲2SJ77Ⓚ(10) △2SK196Ⓗ(8)					○2SK135(1.0) ○2SJ50(1.0)	○2SK220Ⓗ(1.0)
180	▲2SK215(8) ▲2SJ78(10)		▲2SK408(7.0) ▲2SK409(7.0)	▽2SK318(1.9)			○2SK175(1.0) ○2SJ55(1.0) ▽2SK317(0.95) ▽2SK410(1.2)
200	▲2SK216(8) ▲2SK216Ⓚ(8) ▲2SK79(10) ▲2SJ79Ⓚ(10)						○2SK176(1.0) ○2SJ56(1.0) ○2SK221Ⓗ(1.0)
250							○2SK258Ⓗ(0.8)
350					○2SK259Ⓗ(2.5)		
400					○2SK260Ⓗ(2.5)		

Note 1.* : Under Development

( ) : $R_{DS(on)typ}$

Note 2. Package

□ DPAK ● TO-3P

■ TO-126 ○ TO-3

△ TO-39 ▽ RFPAK

▲ TO-220AB

Table 3-3 Typical Characteristics of Power MOS FET D-series

Package	Type Number		Absolute Max. Ratings				Electrical Characteristics					
	N—ch	P—ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	Pch** (W)	$R_{DS(on)}$(Ω) typ	$R_{DS(on)}$(Ω) max	$\|y_{fs}\|$* (S)	ton (ns)	toff (ns)	fc (MHz)
DPAK	2SK416	2SJ120	40	±20	2	10	0.5/1.2	0.8/1.5	0.4/0.25	25/35	35/40	25
	2SK429	—	100		3	20	0.5	0.7	0.9	35	50	5
	2SK430	—	150				0.8	1.0				
	2SK375	—	300		1	10	2.5	4.0	0.4	20	70	10
	2SK535	—	400		1.5	20	4.0	6.0	0.4	20	45	10
	2SK384	—	500		0.3	10	25	50	0.1	20	20	40
TO—126	2SK511	—	250	±9	0.3	8	30	50	0.08	—	—	250
TO—220AB	2SK345	2SJ101	40	±20	5	30	0.3	0.4	0.9	40/60	70/100	7
	2SK346	2SJ102	60									
	2SK428	2SJ122			10	50	0.1/0.15	0.15/0.2	2.2	60/80	120/200	3
	2SK294	—	80		5	30	0.4	0.56	0.8	40	70	5
	2SK295	—	100									
	2SK383	—			10	50	0.15	0.18	2.8	60	150	4
	2SK440	—	200		6	40	0.4	0.5	1.8	40	110	3
	2SK296	—	300		1	30	2.5	4.0	0.4	20	70	10
	2SK310	2SJ117	400		3/2	40	2.5/5.0	4/7	1.0/0.7	25/35	70/80	10
	2SK311	—	450		3		2.5	4.0	1.0	25	70	10
	2SK319	—	400		5	50	1.1	1.83	1.5	50	120	5
	2SK320	—	450									
	2SK382	—	500		2	30	2.5	4.0	0.7	25	70	10
	(2SK513)	—	800		3	60	5.0	6.0	0.7	50	120	5
TO—3P	2SK399	2SJ113	100	±20	10	100	0.2/0.25	0.25/0.35	2.0	50/70	110/160	3
	2SK413	2SJ118	140		8		0.4	0.5	2.0/1.8	50/70	110/160	3
	2SK414	2SJ119	160									
	2SK400	2SJ114	200				0.5/0.6	0.7/0.8	1.8	40/50	110/160	3
	2SK412	—	250		10		0.3	0.4	2.5	65	180	3
	2SK402	—	400		8		1.1	1.75	1.7	50	120	5
	2SK403	—	450									
	2SK349	—	400		10		0.67	0.9	2.5	70	200	3
	2SK350	—	450									
	2SK415	—	800		3	80	5.0	6.0	0.7	50	120	5
	2SK534	—			5	100	3.0	4.0	1.2	75	220	4
TO—3	2SK398	2SJ112	100	±20	10	100	0.2/0.25	0.25/0.35	2.0	50/70	110/160	3
	2SK308	—	120				0.2	0.3	2.8	60	160	4
	2SK401	—	250				0.3	0.4	2.5	65	180	3
	2SK298	2SJ116	400		8	100/125	1.1/1.75	1.75/2.25	1.7/1.6	50/60	120/220	5/3
	2SK299	—	450			100	1.1	1.75	1.7	50	120	5
	2SK312	—	400		12	125	0.67	0.9	2.5	70	200	3
	2SK313	—	450									
	2SK512	—	500				0.55	0.65	3.5	75	300	—
	2SK351	—	800		5	125	1.7	3.0	2.0	100	300	2

Note ( ) : Under Development (The specifications subject to change without notice.)

* : Test Condition $V_{DS} > I_D \times R_{DS(on)}$, $I_D \fallingdotseq \frac{1}{2} I_{Dmax}$(DC)

** : Value at Tc=25°C

Table 3-4 Typical Characteristics of Power MOS FET S-series

Package	Type Number		Absolute Max. Ratings				Electrical Characteristics					
							$R_{DS(on)}$ (Ω)		*** $\|y_{fs}\|$ (S)	ton (ns)	toff (ns)	fc (MHz)
	N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	Pch** (W)	typ	max				
TO-220 AB	2SK213	2SJ76	140*	±15	0.5	30	8/10	—	0.15/0.1	20	30	40/30
	2SK214	2SJ77	160*									
	2SK214Ⓚ	2SJ77Ⓚ	160*									
	2SK215	2SJ78	180*									
	2SK408,409	—	180	±20	2.0	30	7	9	0.3	—	—	200
	2SK216	2SJ79	200*	±15	0.5	30	8/10	—	0.15/0.1	20	30	40/30
	2SK216Ⓚ	2SJ79Ⓚ	200*									
TO-39	2SK196Ⓗ	—	160	±15	0.5	0.8	8	15	0.15	20	30	30
TO-3	2SK133	2SJ48	120*	±14	7	100	1.0	1.7	1.0	180/230	60/110	3/2
	2SK134	2SJ49	140*									
	2SK135	2SJ50	160*									
	2SK175	2SJ55	180*	±20	8	125	1.0	1.7	1.0	250/320	90/120	2/1
	2SK176	2SJ56	200*									
	2SK176Ⓗ	2SJ56Ⓗ	200							60	200	
	2SK220Ⓗ	—	160	±20	8	100	1.0	1.5	0.9	25	45	50
	2SK221Ⓗ	—	200									
	2SK258Ⓗ	—	250		8	125	0.8	1.1	1.3	25	140	7
	2SK259Ⓗ	—	350		5	125	2.5	3.0	1.0	25	140	7
	2SK260Ⓗ	—	400									
RFPAK	2SK317	—	180	±20	8	120	0.95	1.25	125	—	—	300
	2SK318	—			4	70	1.9	2.5	0.6			
	2SK410	—			8	120	1.2	1.5	1.25	—	—	350

Note * : V_{DSX}

** : Value at Tc=25°C

*** : Test Conditions $V_{DS} > I_D \times R_{DS(on)}$, $I_D \fallingdotseq I_{Dmax(DC)}$

● Power MOS FET DII Series

Hitachi achieved development of high-performance new Power MOS FET Series (DII Series) by original technique. 15 types of DII series in the below table are going to be in production.

DII series have the following features;

. High gain (gm is 2 ~ 3 times higher than that of current D series.)

. Low On-resistance (Ron is 30 ~ 50% lower than that of Current D series.)

The maximum rated current can be driven by low input voltage: 7 ~ 8V due to high gm. Driving power needs only 1/3 ~ 1/4 of that of current D series (at V_{GS}=10 ~ 15V) so that this series gives more energy saving in the circuit.

Table 3-5 Typical Characteristics of Power MOS FET DII Series

Package	Type Number		Absolute Max. Rating				Electrical Characteristics					
	N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_D (W)	R_{DS}(on) (Ω) typ.	R_{DS}(on) (Ω) max.	|Yfs| (S)*	t_{on} (ns)	t_{off} (ns)	f_c (MHz)
DPAK	2SK579	-	450	±15	1.5	20	3.5	5.5	1.0	28	48	15
	2SK580	-	500				4.0	6.0				
TO-220AB	2SK549	-	60	±15	10	50	0.1	0.15	5.0	55	100	3
	2SK600	-	60		25	75	0.04	0.055	15	115	245	1.5
	2SK551	(2SJ127)	120		10	50	0.15/0.2	0.2/0.25	5/5	55/110	100/240	3
	2SK552	-	450		5	50	1.0	1.4	4.0	45	115	2
	2SK553	-	500				1.2	1.5				
	2SK554	-	450		7	60	0.6	0.85	6.5	65	155	1.5
	2SK555	-	500				0.7	1.0				
TO-3P	2SK556	-	450	±15	12	100	0.40	0.55	10	110	230	1
	2SK557	-	500				0.45	0.6				
	2SK559	-	450		15	100	0.25	0.36	13	145	320	
	2SK560	-	500				0.3	0.4				
TO-3	2SK561	-	100	±15	30	150	0.05	0.07	15	110	240	1.5

Note ( ): Under Development (The specifications subject to change without notice)

* : Test Condition $V_{DS} \geq I_D \times R_{DS}(on)$, I_D=1/2 I_D max(DC)

● Power MOS FET Module

Nowadays, high power transistors tend to be in module package, especially in the field of motor control. On the other hand, power MOS FETs, because of their superior response, has begun to be applied to robots and manufacturing machines to improve their performance. In order to meet these requirements, Hitachi has developed power MOS FET modules. Table 3-6 shows their typical characteristics.

Table 3-6 Typical Characteristics of Power MOS FET Modules

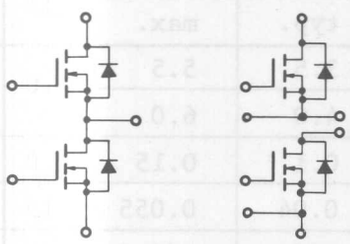
Package	Type Number	Absolute Maximum Ratings				Electrical Characteristics					Equivalent Circuit
		V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}** (W)	$R_{DS(on)}$(Ω) typ	$R_{DS(on)}$(Ω) max	$\|y_{fs}\|$ (S)	ton (ns)	toff (ns)	
B	PM1210B	120	±20	10	50	0.2	0.3	2.0	60	160	1
	PM1220B	120	±20	20	80	0.1	0.15	4.0	120	320	
C	PM4550C	450	±20	50	300	0.13	0.18	12	350	1000	2
	(HS7910)	500	±20	50	300	0.12	0.16	18	550	1500	
F	(HS7920)	500	±20	30	150	0.2	0.27	10	350	900	2

Note 1) ( ) : Under Development (They are subject to change without notice.)

* : Per one transistor

** : Value at Tc=25°C

2) Internal equivalent circuit



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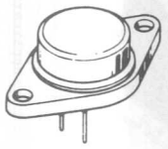
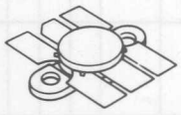
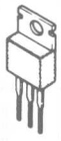
• Power MOS FET

Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)
TO-3	100~800	5~30	0.05~3.0
TO-3P	100~800	3~15	0.2~5.0
TO-220	40~800	1~25	0.03~5
DPAK	40~500	0.3~3.0	0.5~25

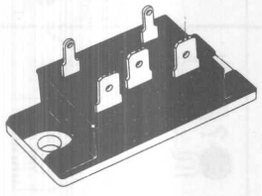
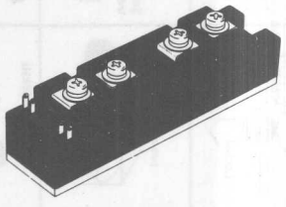
Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)
TO-126	250	0.3	30
RFPAK	180	4 , 8	0.95~1.9
TO-39	160	0.5	8




• Power MOS FET Module

Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)
B	120	10~20	0.1~0.2
C	450~500	50	0.12~0.13

3.2 Application of Power MOS FET

Table 3-7 shows the applications and recommended types of each power MOS FET.

Table 3-7 Applications

Applications	Features: Bipolar transistor	Features: Power MOS FET	Function		Type Number: DPAK	TO-126	TO-220	TO-3P	TO-3	RFPAK	Module
Audio output	DC power, Output, Loss (Heat) (Large)	DC power, Output, PWM, Loss (little)	Linear power amplifier				2SK214 2SJ77 2SK216 2SJ79	2SK413 2SJ118 2SK400 2SJ114	2SK134 2SJ49 2SK175 2SJ55		
			PWM amplifier				2SK346 2SJ102 2SK428 2SJ122 2SK551 (2SJ127)	2SK399 2SJ113 2SK413 2SJ118 2SK400 2SJ114			
High speed power switching circuit	f=20~50kHz	f=100~500kHz Small size light weight	Switching power supply	AC 100V	2SK535 2SK579 2SK580		2SK310 2SK319 2SK552 2SK554	2SK402 2SK349 2SK556 2SK559	2SK298 2SK312		
				AC 200V			2SK513	2SK415 2SK534			
				Input DC 12~24V	2SK429 2SK430		2SK383 2SK551	2SK399	(2SK561)		
				Input 48V			2SK440	2SK400 2SK412	2SK401		
	f=1~20kHz	f=200~500kHz High frequency, High speed manufacturing	Arcing machine Laser beam machine					2SK350 2SK557 2SK560	2SK313 2SK512 2SK351		PM4550C (HS7910)
Motor control		High controllability	Servo-motor				2SK383	2SK414 2SJ119 2SK412	2SK308 2SK401		
			Stepping motor				2SK346 2SJ102 2SK428 2SJ122 2SK319	2SK413 2SK118 2SK400 2SJ114	2SK312 2SJ116 2SK557		
			Inverter				2SK320 2SK554	2SK350 2SK557	2SK312 2SJ116 2SK557		(HS7910)
Ultrasonic application	f=2~8MHz	Clear f=10 MHz	Ultrasonic diagnostic system Fish finder Ultrasonic washer		2SK375 2SK535 2SK579 2SK580		2SK296 2SK310 2SK311 2SK382 2SJ117				
Telecommunication equipment	Power supply	Small size Easy maintenance Save power Power supply	Medium and short waves				2SK408 2SK409		2SK176 2SK221 ⊕ 2SK258 ⊕ 2SK260 ⊕	2SK410	
			FM, VHF band							2SK317 2SK318 2SK410	
			MCA Personal radio communication								PF0002*
Others (Tubes and display)	Video band 10~20MHz	Video band 40~80MHz High Resolution	Tube, Display			2SK511					
			Coil drive		2SK416 2SJ120						
			Relay analog switch		2SK384 2SK580		2SK549 2SK600				

Note 1) ( ) : Under development
2) * : Outline

3) The types shown above are used for the underlined applications in the table.

4.APPLICATION HINTS

4.1 Audio Power Amplifier

4.1.1 Linear Power Amplifier

(1) Design of output stage (Design of power supply voltage V_{DD})

Fig. 4-1 shows an equivalent circuit of the output stage. R_{ON} is a drain-to-source equivalent resistance when the power MOS FET is on, and according to the 2SK134/2SJ49 spec, it is;

$$R_{ON} = \frac{V_{DS(sat)}}{I_D} = \frac{12}{7} = 1.71\,\Omega$$

The peak current I_p flowing through load R_L=8Ω at Po=100W is calculated from mean current I,

$$P_O = I^2 R_L$$

$$I_p = \sqrt{2} \cdot I = \sqrt{\frac{2P_O}{R_L}}$$

$$= \sqrt{\frac{200}{8}} = 5\ A$$

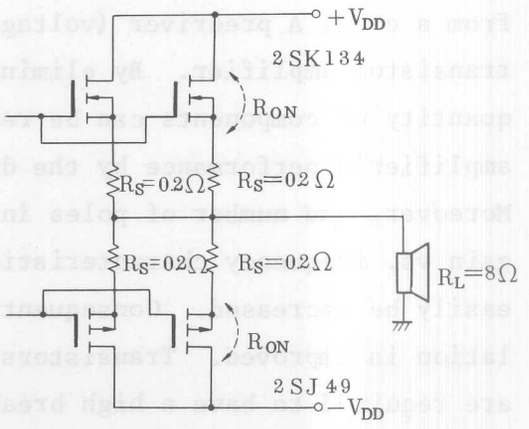


Fig. 4-1 Equivalent Circuit of the Output Stage

Therefore, if the transformer regulation is estimated at 20% and the AC line regulation at ±15%, then the power supply voltage V_{DD} is given as;

$$V_{DD} = 1.2 \times 1.15 \left\{ R_L + \frac{(R_{ON} + R_S)}{2} \right\} I_p$$

$$\fallingdotseq 61.8\ V$$

In Fig. 4-3, the power supply of power stage is common with that of voltage amplifier stage, so the voltage is set at ±65V including the gate-to-source ON voltage at Po=100W.

In the case of D series 2SK343/2SJ99, the R_{ON} value is very small (0.5Ω), the supply voltage required for the same output (100W) is only 57.6V. This enables us to make the transformer capacity and the cooling fin smaller, resulting in cost reduction.

(2) Design of voltage amplifier stage

A power MOS FET can be driven by a low driving power. Fundamentally, only power for charging and discharging the gate-to-source capacitance is needed by the output stage, so that a class B driver stage is not required. The driving power varies with input frequency. At 100W output and 100kHz frequency, it would be very small as follows.

$$Pin = f \cdot Ciss \cdot V_{GS}{}^2 = 100 \times 10^3 \times 900 \times 10^{-12} \times 6^2 = 3.24\,mW$$

Therefore, an output stage power MOS FET can be driven directly from a class A predriver (voltage amplifier stage) used in a bipolar transistor amplifier. By eliminating the class B driver, the quantity of components can be reduced, and impairment of the amplifier's performance by the driver itself can be avoided. Moreover, the number of poles in the transfer function (open loop gain vs. frequency characteristics) decreases, and the stagger can easily be increased. Consequently, the stability against oscillation is improved. Transistors for the voltage amplifier stage are required to have a high breakdown voltage, low Cob (collector output capacitance) and high f_T (gain-bandwidth product).

(3) Open loop voltage gain

The transconductance $|y_{fs}|$ of power MOS FETs is as large as 1.0 ∿ 2.5S typ. Yet it is only a fraction of that of bipolar transistors. For example, $|y_{fs}|$ of bipolar transistors at I_C (collector current)= 1.0A, is very large, as follows;

$$|y_{fs}| = \frac{1}{r_e} = \frac{I_E}{KT/q} = \frac{1\,A}{26\,mV} \fallingdotseq 38\,S$$

where re: Emitter equivalent resistance
K: Boltzmann constant
T: Absolute temperature
q: Electron charge
I_E: Emitter bias current

When the power device is used in the source follower (In bipolar transistor circuit; it's called emitter follower), the relationship between input and output is;

$$\frac{\text{output}}{\text{input}} \fallingdotseq \frac{R_L}{R_L + 1/|y_{fs}|}$$

(See Fig. 4-2)

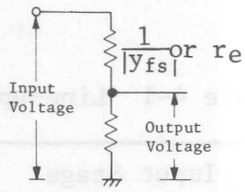


Fig. 4-2 Source Follower Input & Output

Only the nonlinear component of this equation, $1/|y_{fs}|$, causes distortion, so that a larger $|y_{fs}|$ is of lower distortion. In other words, since a power MOS FET amplifier has a distortion about 20dB larger than a bipolar transistor amplifier, it is necessary to design for larger open loop gain and larger negative feedback than in a bipolar transistor circuit.

(4) Considerations for parasitic oscillation

Because power MOS FETs have excellent high-frequency characteristics, they are liable to cause oscillation, even in a simple circuit.

For an analysis of stability in a source follower circuit, see paragraph 5.9 of Power MOS FET Data Book (MAR, 1985). Here, we would like to show some precautions in fabrication.

- Minimize the wiring between the printed circuit board and the power MOS FETs. Direct connection is recommended.
- Provide one-point grounding for the amplifier printed circuit, power supply, and speaker terminals. Make the wiring of power supply line and ground line as big as possible.
- The output coupling coil L has the effect of reducing distortion in the high frequency range. It also prevents oscillation which might occur when the output is loaded by capacitance.
  Its value should be determined experimentally.
- Printed circuit layout should flow topographically from input to output.

(5) Line up

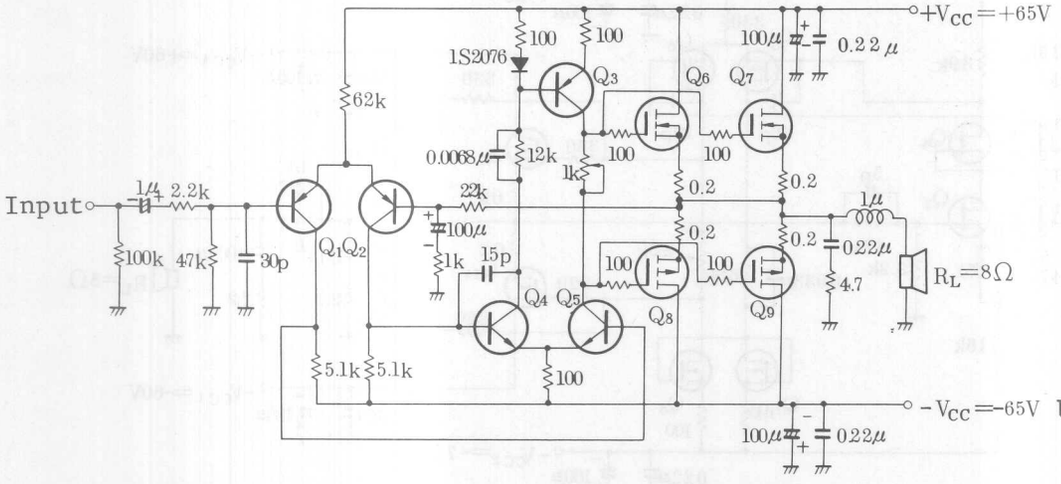
Table 4-1 Line-up of Devices in Audio Amplifier

Output Power		Input Stage			Driver Stage				Output Stage	
			Bipolar		FET (V_{DSX})		Bipolar (V_{CEO})		FET (V_{DSX})	
Single Pushpull	Parallel Pushpull	FET	NPN	PNP	N Channel	P Channel	NPN	PNP	N Channel	P Channel
50~60	—	2SK190 2SK186	2SC1775 2SC2855	2SA872 2SA1190	2SK213 (140V)	2SJ76 (−140V)	2SD756 (120V)	2SB716 (−120V)	2SK133 (120V)	2SJ48 (−120V)
60~80	100~120				2SK214 (160V)	2SJ77 (−160V)	2SD756A (140V)	2SB716A (−140V)	2SK134 (140V) 2SK413 (140V)	2SJ49 (−140V) 2SJ118 (−140V)
—	120~140	—			2SK215 (180V)	2SJ78 (−180V)	2SD668A (160V)	2SB648A (−160V)	2SK135 (160V) 2SK414 (160V)	2SJ50 (−160V) 2SJ119 (−160V)
80~100	—				2SK216 (200V)	2SJ79 (−200V)	2SD758 (200V)	2SB718 (−200V)	2SK175 (180V)	2SJ55 (−180V)
—	140~200	—	2SC1775A 2SC2856	2SA872A 2SA1191	—	—			2SK400 (200V) 2SK176 (200V)	2SJ114 (−200V) 2SJ56 (−200V)

Underline is D Series (Drain Case Type)

(6) Application Circuit

● 100W Output THD≒0.01%, f=100kHz



Q_1, Q_2 : 2SA872
Q_3 : 2SB716A
Q_4, Q_5 : 2SD756A
Q_6, Q_7 : 2SK134
Q_8, Q_9 : 2SJ49

Unit R : Ω
C : F
L : H

Fig. 4-3 P_O=100W Power Amp. Circuit Diagram

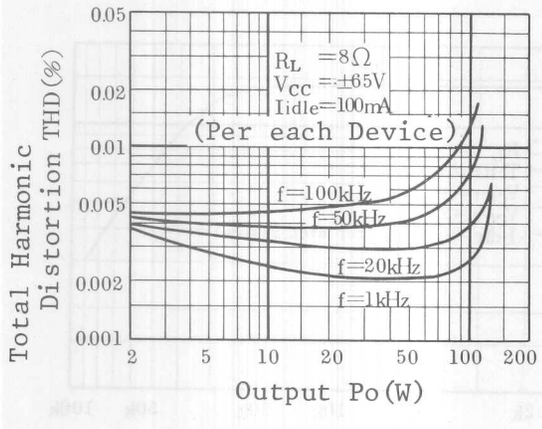


Fig. 4-4 Total Harmonic Distortion vs. Output Characteristics

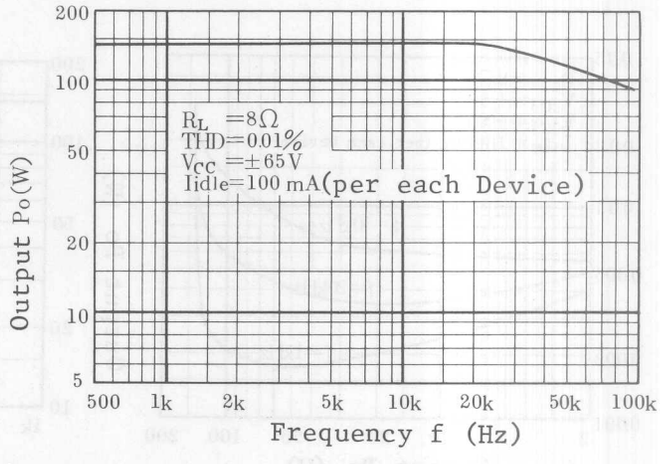


Fig. 4-5 Power Band Width

● 100W Output THD≒0.01%, f=50kHz
(All FET DC Amplifier)

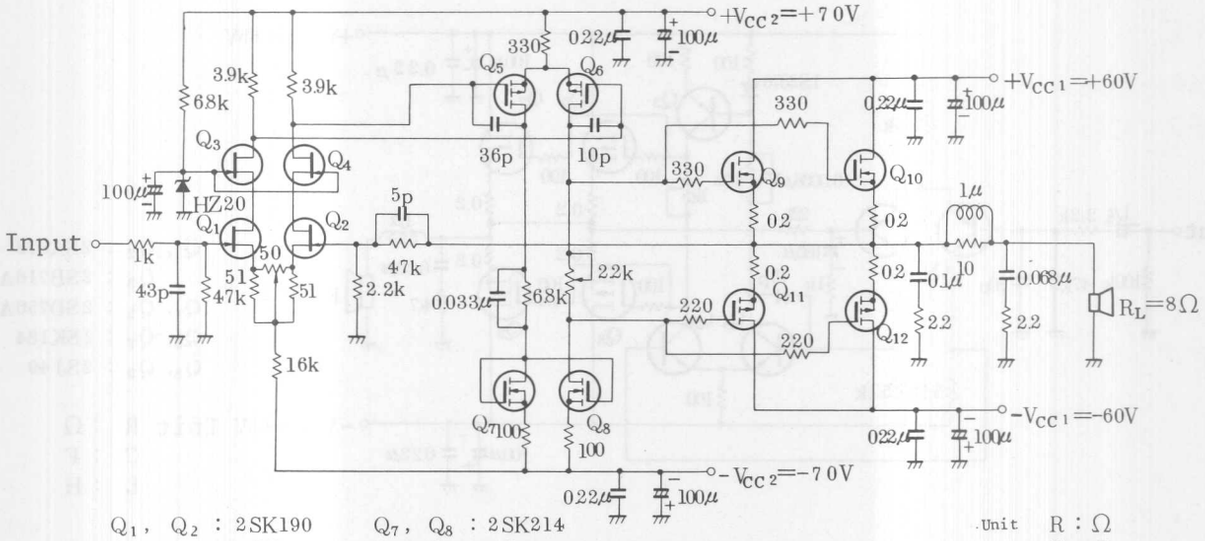


Fig. 4-6 Po=100W All FET Power Amp. Circuit Diagram

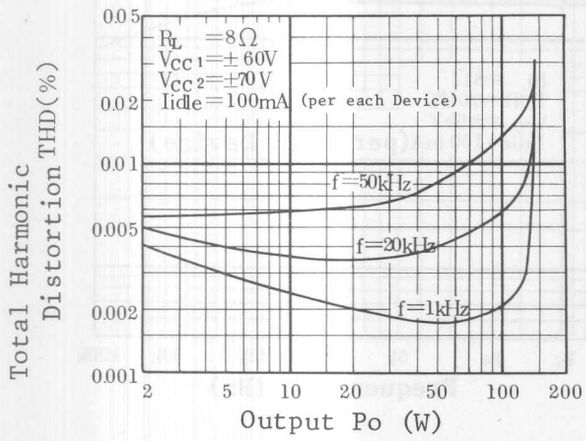


Fig. 4-7 Total Harmonic Distortion vs. Output Characteristics

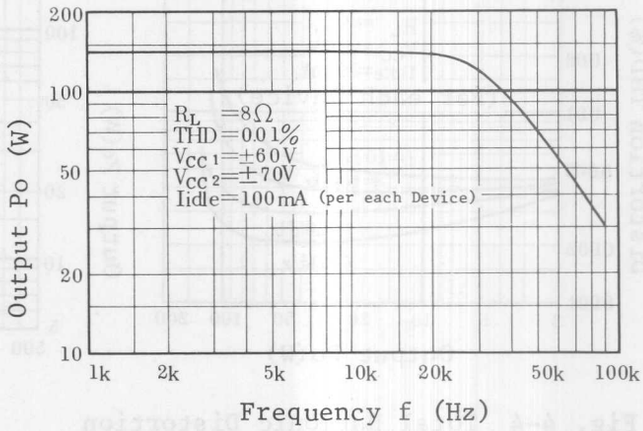


Fig. 4-8 Power Band Width

4.1.2 PWM Amplifier

The PWM (Pulse Width Modulation) Amplifier is a signal reproducing system in which a input signal is converted to a pulse signal whose width or duty cycle is proportional to the input signals amplitude. This variable duty cycle but constant amplitude signal is amplified, low pass filtered, and then applied to the load, losses are primarilly switching losses in the output devices. This allows a very high output power with very small physical size.

The most important characteristic required for a output device in a PWM amplifier is high switching speed. The t_{off} speed of a bipolar transistor is slower than that of a power MOS FET of similar power rating. The t_{off} ($t_{off}=t_{d(off)}+t_f$) value of a power MOS FET is only 100 ∿ 200ns, giving it an advantage in PWM switching operation of several hundred kHz.

(1) Theory & Block Diagram of PWM Amplifier

Fig. 4-9 and Fig. 4-10 show the block diagram and the waveform of a PWM amplifier.

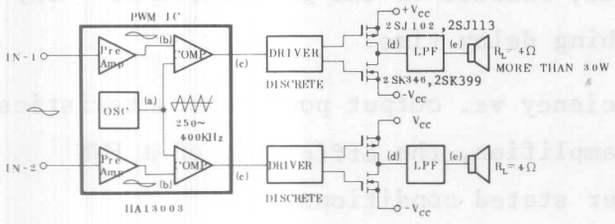


Fig. 4-9 PWA Amp. Block Diagram

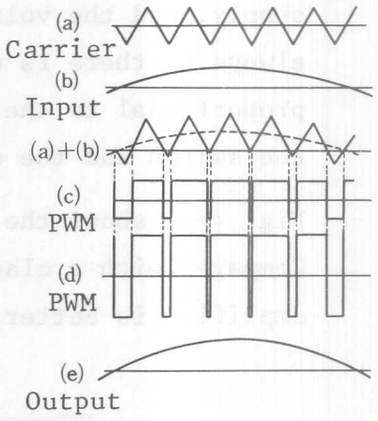


Fig. 4-10 Waveform

In this PWM amplifier, the input signal (b) is added to the carrier signal (a) (a triangular wave) through a comparator, and then that signal ((a) + (b)) is converted to a pulse signal whose pulse width is proportional to the input signal level. This means that the pulse duty cycle is proportional to the input signal level.

The pulse signal (c) drives the output power devices. The power devices switch the power supply, and the resulting output power is passed to a low pass filter (hereinafter referred to as LPF). The original signal input (b) is reproduced amplified (e) at the output of the LPF.

When the frequency of carrier signal (a) is higher, the quantity of information is more accurate and the distortion is lower. According to information theory, if the frequency is more than twice as high as the maximum transmission frequency, the original frequency can be reproduced. In the PWM amplifier, however, the distortion will be worse, because the lower side band is mixed into the audio signal. Therefore, if the maximum transmission frequency is 20 ∿ 50kHz, the carrier frequency should be normally 200 ∿ 500kHz (5 ∿ 10 times).

(2) Power Efficiency of PWM Amplifier

In a class-B amplifier, the amplification device operates as a resistance, so the device loss is large. On the other hand, in a PWM amplifier, since the switch is connected directly to the power supply, and the voltage-current product in a ideal switch is always 0, there is no loss. In fact, however, there is loss proportional to the output, because of the ON resistance (R_{ON}) of the switch and the switching delay time.

Fig. 4-11 shows the efficiency vs. output power characteristics. Compared with a class-B amplifier, the efficiency of a PWM amplifier is better, under stated conditions.

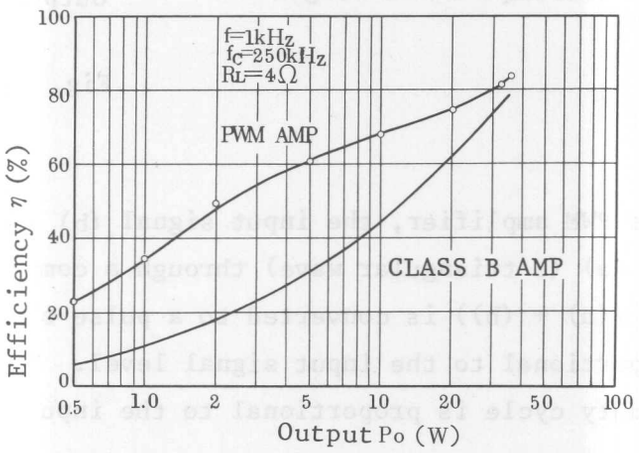


Fig. 4-11 Efficiency vs. Output Characteristics

(3) Relation between output power device and distortion

Distortion in a PWM amplifier occurs, under the influences of; 1) frequency of carrier signal, 2) linearity of triangular wave and 3) attenuation of LPF. In this section, we would like to explain the distortion that occurs at the output stage of the power switching circuit.

Fig. 4-12 shows a PWM output circuit in which power MOS FET's are used, and Fig. 4-13, the operating waveforms.

(a) shows driving voltage waveform (v_i) and (b) ∿ (e), voltage and current waveform at each point. The current can't be changed instantaneously because of the LPF's inductance, resulting in the waveform shown in (e). Examining the current more minutely, from t_1 to t_2, Q_1 is in ON state and forward current (i_1) flows. As soon as the Q_1 turns OFF, a inverse voltage is generated by the LPF's inductance and to absorb it, current (i_2) flows through the Q_2 diode (t_2 ∿ t_3). Then Q_2 turns ON and forward current (i_3) flows (t_3 ∿ t_4). Then current (i_4) flows through the Q_1 diode (t_4 ∿ t_5). The current flows repeating the above operations. Here, the important point is that the current can flow backward. This means that a power MOS FET does not require an external commutating diode because it has an equivalent backward diode. On the other hand, if a bipolar transistor is used in the output stage, an external diode is needed.

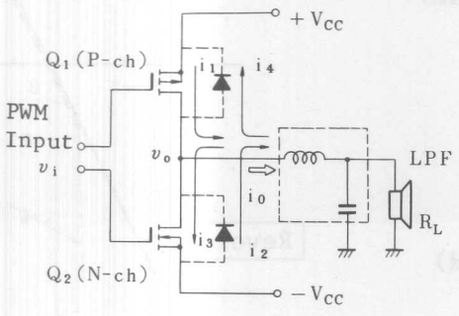


Fig. 4-12 Equivalent Circuit of PWM Output Stage

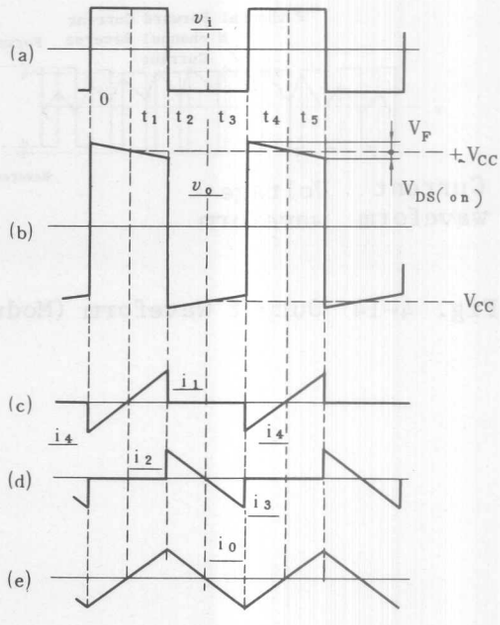


Fig. 4-13 Waveform (Unmodulated)

As for the voltage waveform (V_o), the remaining voltage $V_{DS(on)}$ and the backward diode V_F of power MOS FET cause amplitude fluctuation of the output voltage. Therefore the waveform as shown in (b) is generated, instead of a correct square wave.

When a input signal is supplied, the pulse width is modulated and power is provided to the speaker, the current flown to LPF is as shown in Fig. 4-14. The output waveform is determined like this; if the triangular current is positive, it is determined by the forward current of P channel and the backward current of N channel, and if the triangular current is negative, it is determinend by the forward current of N channel and the backward current of P channel.

As for the MOS FET output characteristics (V_{DS} vs. I_D characteristics), in the standard MOS FET, as shown by the dotted line in Fig. 4-15, the diode characteristics are seen in the reverse area. Because of this non-linear characteristics, the voltage drop of the output pulse is non-linear and a distortion is caused. Therefore a device is required to have the same forward and backward characteristics.

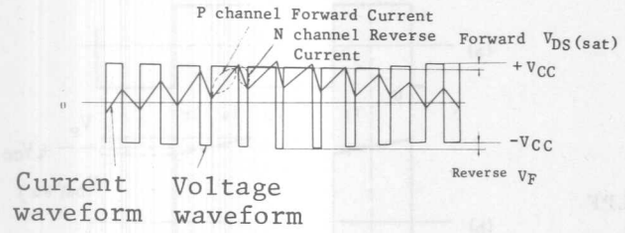


Fig. 4-14 Output Waveform (Modulated)

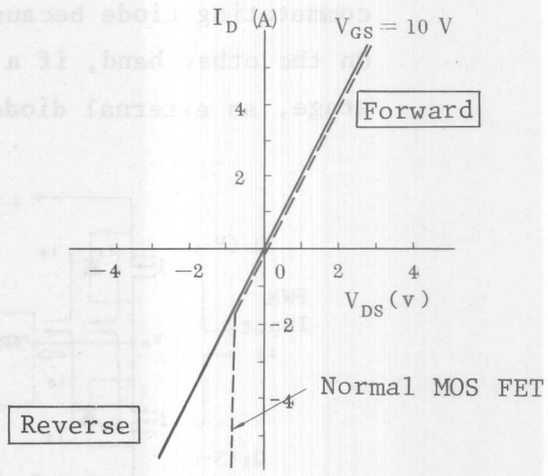
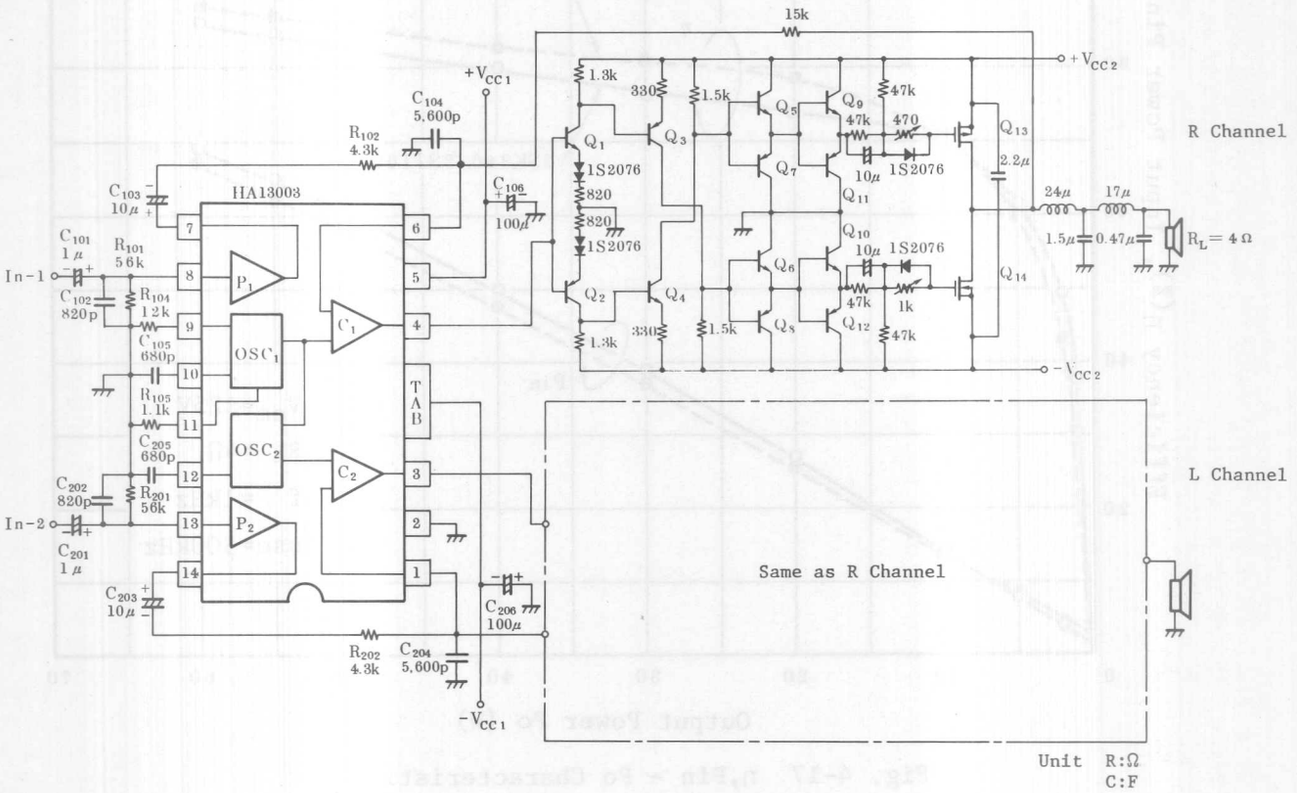


Fig. 4-15 I_D-V_{DS} Characteristics

(4) Application and Line-up



$\pm V_{CC1} = \pm 10V$

$\pm V_{CC2} = \pm 25V$

$fosc \fallingdotseq 300kHz \left(\frac{1}{4 \cdot C_{105} \cdot R_{105}}\right)$

$R_L = 4\Omega$

Q_1, Q_4, Q_5, Q_6 : 2SC2308

Q_2, Q_3, Q_7, Q_8 : 2SA1030

Q_9, Q_{10} : 2SD667

Q_{11}, Q_{12} : 2SB647

Q_{13} : 2SK346, 2SK428

Q_{14} : 2SJ102, 2SJ122

Note

1) As the interference of linking between the switching power MOS FET toward the modulator IC affects the Total Harmonic Distortion and output noise, the electromagnetic shielding over the power MOS FET, its driver circuit and demodulation filter are required.

Fig. 4-16 Po=40~60W PWM Power Amp for Car Stereo

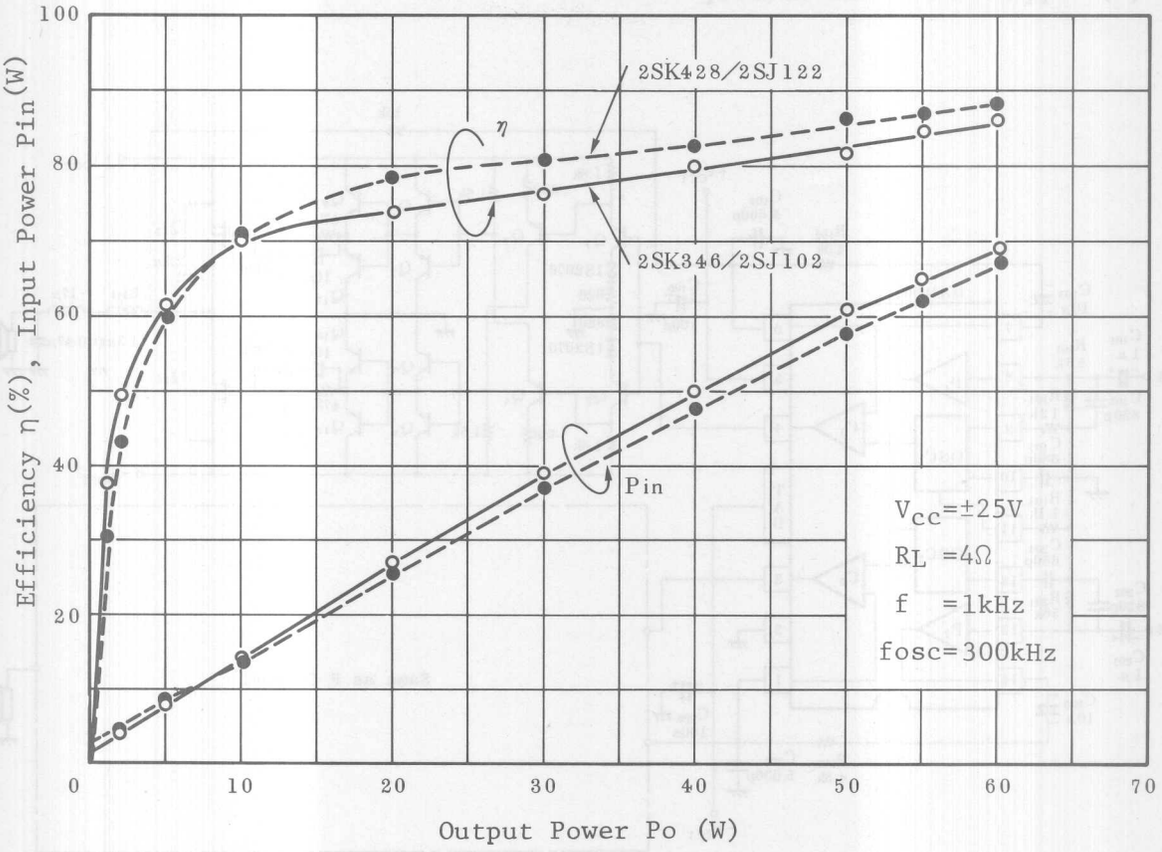


Fig. 4-17 η,Pin - Po Characteristics

Table 4-2 Line-up of Devices for PWM Power Amp

Audio Output Po (W)		Type Number		Package	Absolute Max. Ratings			Electrical Characteristics (typ)		
Single Pushpull	Parallel Pushpull	N-ch	P-ch		VDSS [V]	ID [A]	PD* [W]	RDS(on) [Ω]	ton [ns]	toff [ns]
30~40	—	2SK346	2SJ102	TO-220	60	5	30	0.3	40/60	70/100
40~60	—	2SK428	2SJ122		60	10	50	0.1/0.15	60/80	120/200
60~80	—	(2SK551)	(2SJ127)	TO-220	100	10	75	0.15/0.20	50/70	110/160
		2SK399	2SJ113	TO-3P			100	0.2/0.25		
80~100	—	2SK413	2SJ118	TO-3P	140	8	100	0.4	50/70	110/160
		2SK414	2SJ119		160					

Note

( ) ; Under Development

* ; Tc=25°C

4.2 High Speed Power Switching

4.2.1 Switching Regulator

- Two-transistor Push-pull system 250kHz, 150W (5V, 30A) switching Regulator

Fig. 4-18 shows the block diagram of a two-transistor push-pull system switching regulator in which the 2SK298 is used.

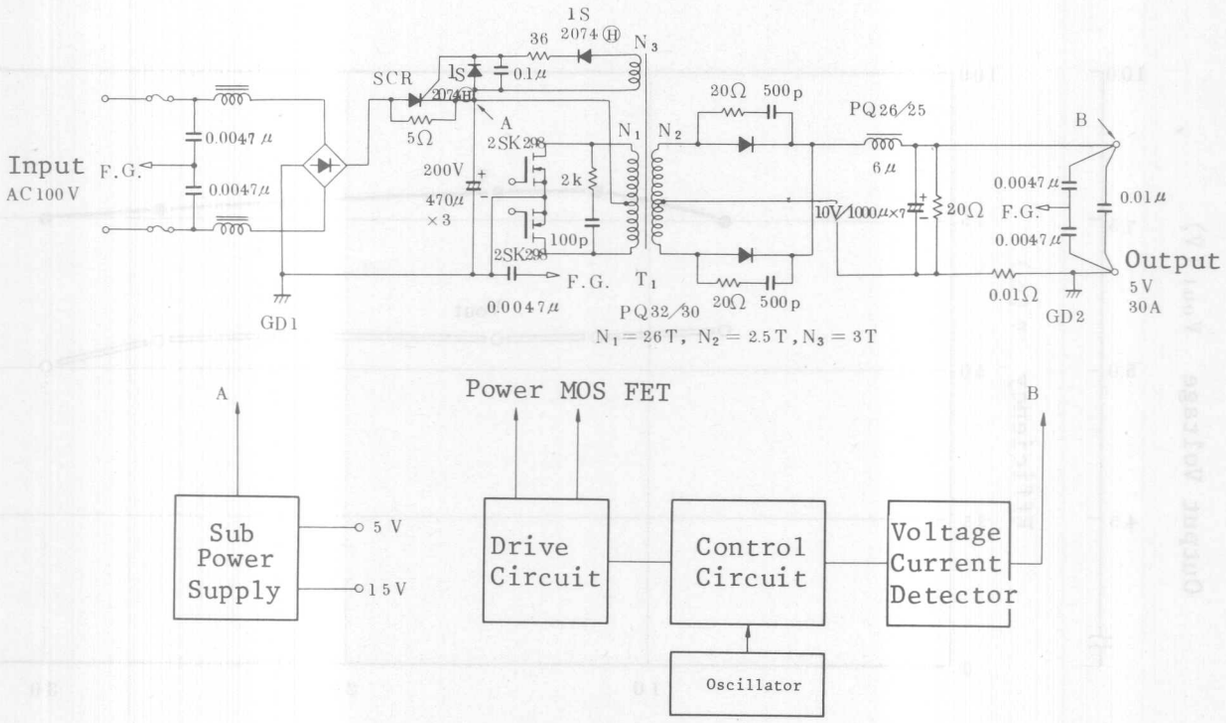
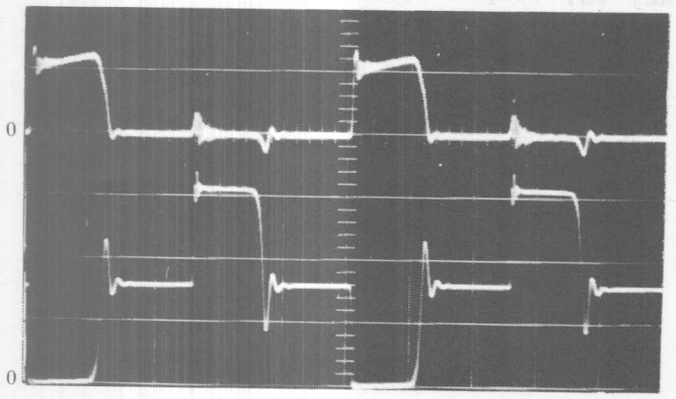


Fig. 4-18 Block Diagram



I_D (2A/DIV)

V_{DS} (50V/DIV)

Fig. 4-19 Waveform for Circuit of Figure 6-16 (Vout=5V, I_D=15A)

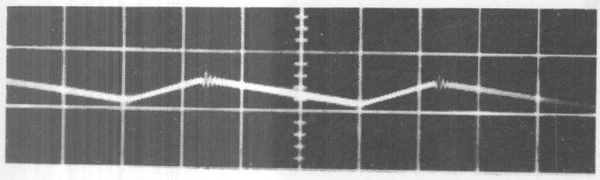


Fig. 4-20 Ripple Waveform of Output Voltage
(V_{out}=5V, I_D=15A)

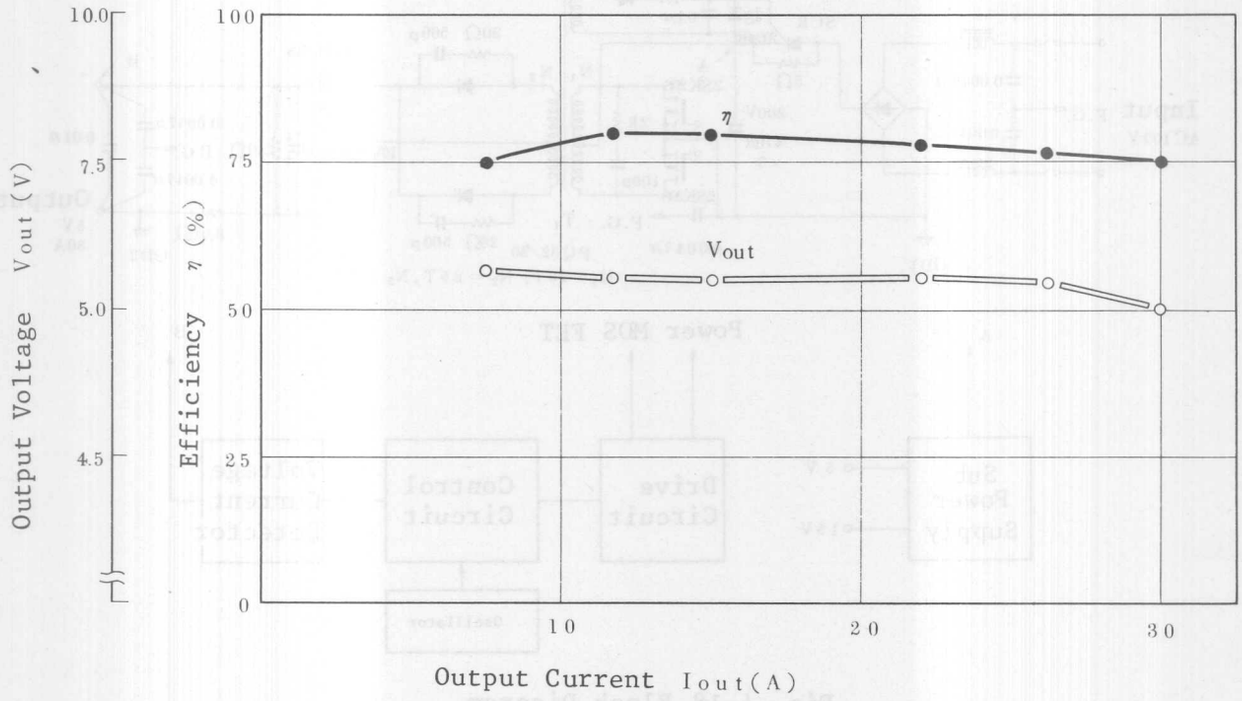


Fig. 4-21 Output and Efficiency vs. Output Current Characteristics

< Circuit Description >

(1) In rush current protection circuit

This circuit is to limit the charging current flowing to the input capacitor when the power supply turns ON. When the sub-power supply circuit turns ON and the main switching transistor (power MOS FET) begins to operate, a voltage is generated at the coil (N_3). By charging capacitor C by the time constant of R and C, the SCR gate is driven. This delay time prevents over current.

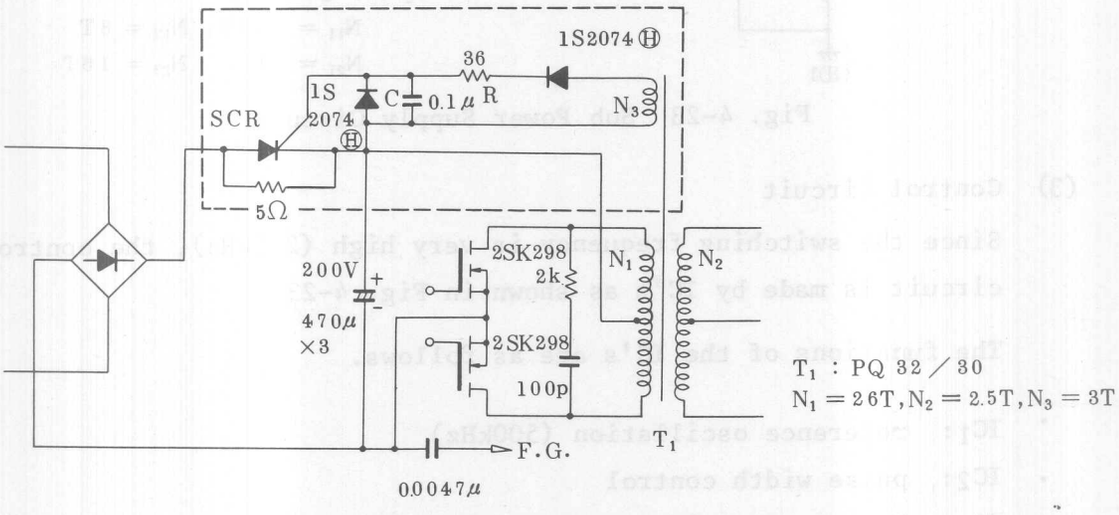


Fig. 4-22 Rush Current Protection Circuit (in dotted line)

(2) Sub Power Supply Circuit

The sub power supply circuit is a blocking oscillator whose secondary output is stabilized by three-terminal regulators; 5V output for IC driving, and 15V output for power MOS FET driving.

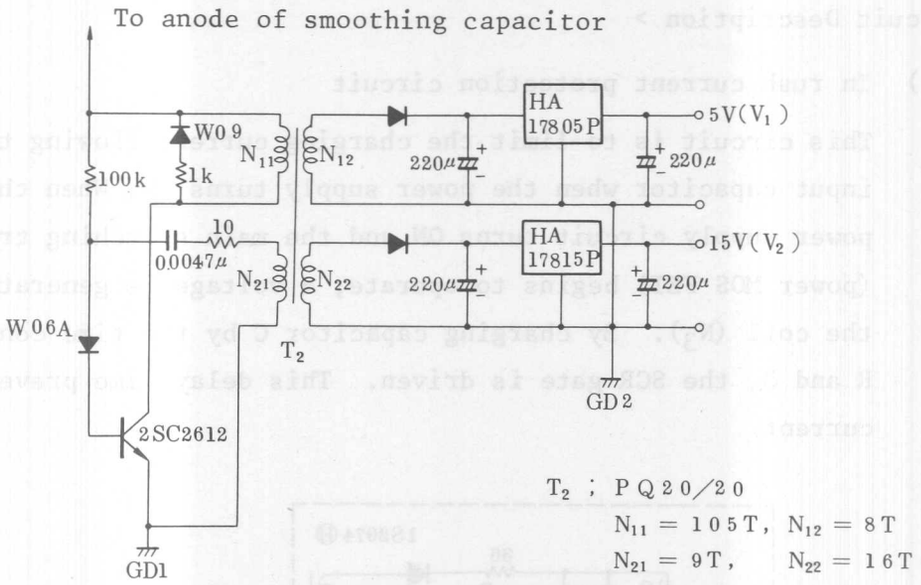


Fig. 4-23 Sub Power Supply Circuit

(3) Control Circuit

Since the switching frequency is very high (250kHz), the control circuit is made by IC's as shown in Fig. 4-23.

The functions of the IC's are as follows.

- IC_1: reference oscillation (500kHz)
- IC_2: pulse width control
- IC_3: 2-phase division
- IC_4: drive output . shut down
- IC_5: voltage detection, detection of over current, detection of over voltage

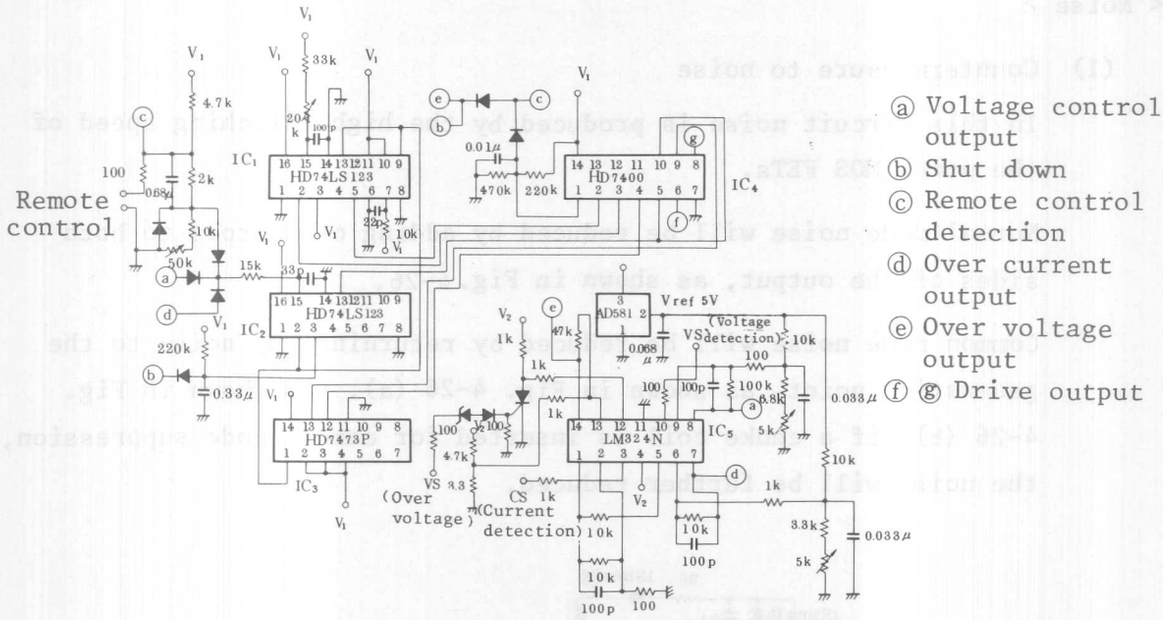


Fig. 4-24 Control Circuit

(4) Drive circuit

The drive circuit is coupled by a pulse transformer for isolation. When T_{r1} is in the ON state, the input capacitance of the power MOS FET is charged through the 330Ω resistance. When T_{r1} turns OFF, T_{r2} is turned ON by the flyback voltage and the input capacitance is discharged by the 51Ω resistance.

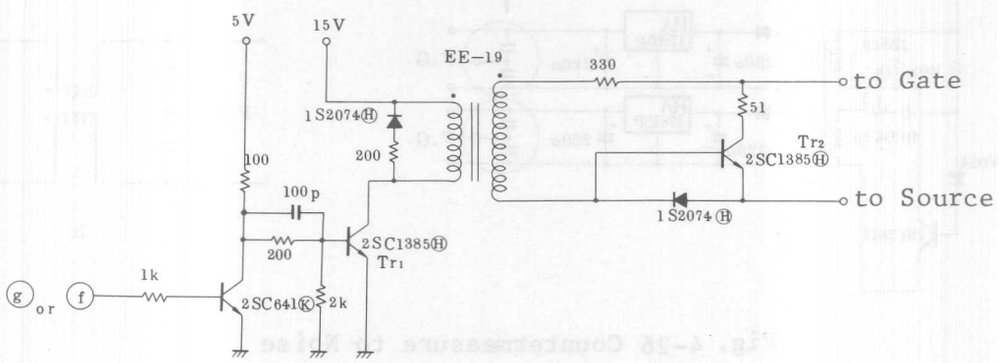


Fig. 4-25 Drive Circuit

< Noise >

(1) Countermeasure to noise

In this circuit noise is produced by the high switching speed of the power MOS FETs.

Normal mode noise will be reduced by adding capacitors to both sides of the output, as shown in Fig. 4-26.

Common mode noise will be reduced by returning the noise to the generation point, as shown in Fig. 4-26 (a). As shown in Fig. 4-26 (b), if a choke coil is inserted for common mode suppression, the noise will be further reduced.

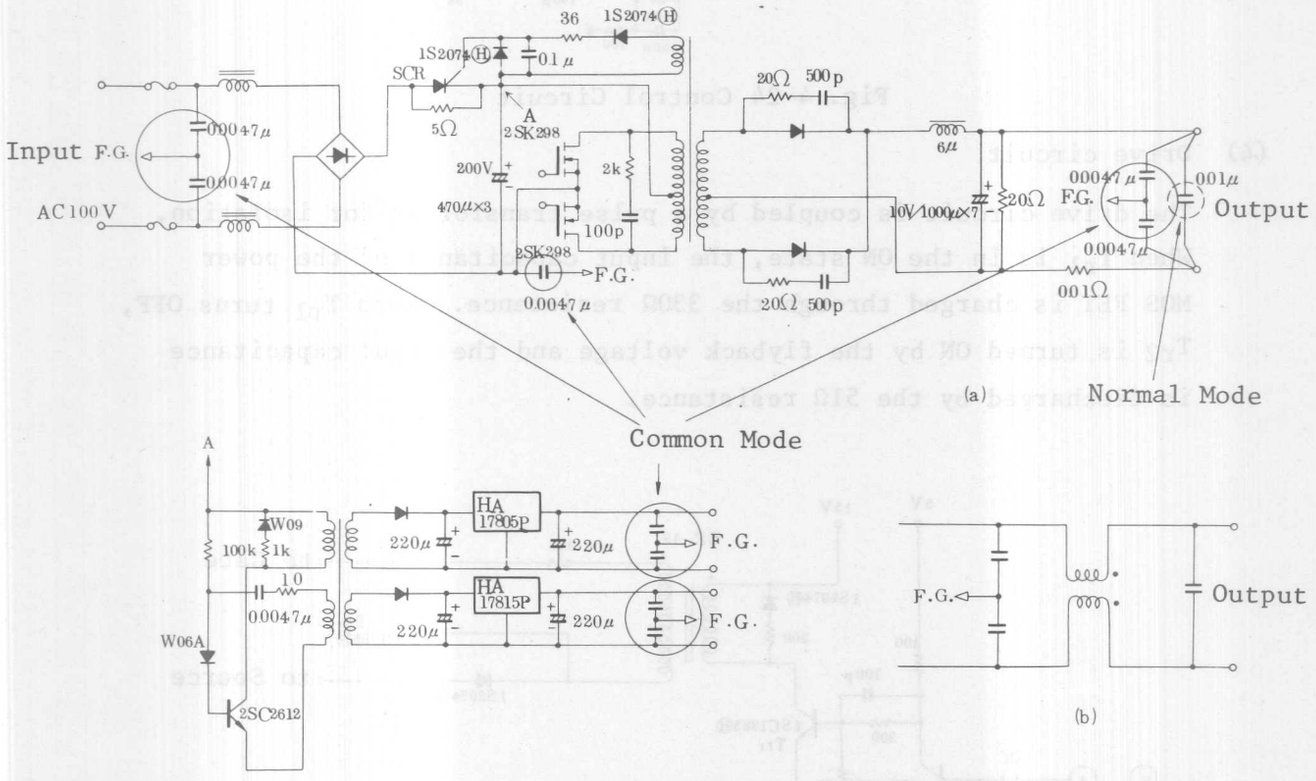


Fig. 4-26 Countermeasure to Noise

(2) Drive Circuit and Noise

As described in the preceding section (1), noise is generated because of the high speed operation of the power MOS FETs. Especially, the ON time has large influence on noise generation. This means that noise can be reduced by improving the drive circuit.

Table 4-3 Drive Circuit and Noise

Item \ Gate Circuit	① R_1, $R_1 \leq rg$	② C_{gd}, R_1	③ R_1, $R_1 > rg$	④ D_1, R_1	⑤ D_1, C_1, R_1, R_2
Parameter	$R_1 = 51\Omega$	$C_{gd} = 50$ pF $R_1 = 51\Omega$	$R_1 = 551\Omega$	$R_1 = 551\Omega$	$C_1 = 300$ pF $R_1 = 551\Omega$ $R_2 = 300\Omega$
Turn-On Time (ns)	30	130	90	90	120
Turn-Off Time (ns)	280	1550	670	280	280
Output Noise (mV) p-p	570	140	135	110	100
Switching Loss (W)	2.7	30.5	6.6	3.0	4.14
Remarks	Switching Loss;Small Switching Time;Small Noise ;Large	Switching Loss;Maximum Switching Time;Large Noise ;Small	Switching Loss;Large Turn Off Time ;Large Noise ;Small	Switching Loss;Small Turn Off Time ;Small Noise ;Small Selection of a constant ;Difficult	Switching Loss;Small Turn Off Time ;Small Noise ;Small

Test Conditions : Input AC 100V, Output 5V · 10A,
Switching Frequency 100 kHz

- ONE TRANSISTOR FORWARD SYSTEM, 500kHz, 50W (5V, 10A) SWITCHING POWER SUPPLY

Fig. 4-27 and Fig. 4-28 respectively show the switching power supply circuit block diagram and its waveforms.

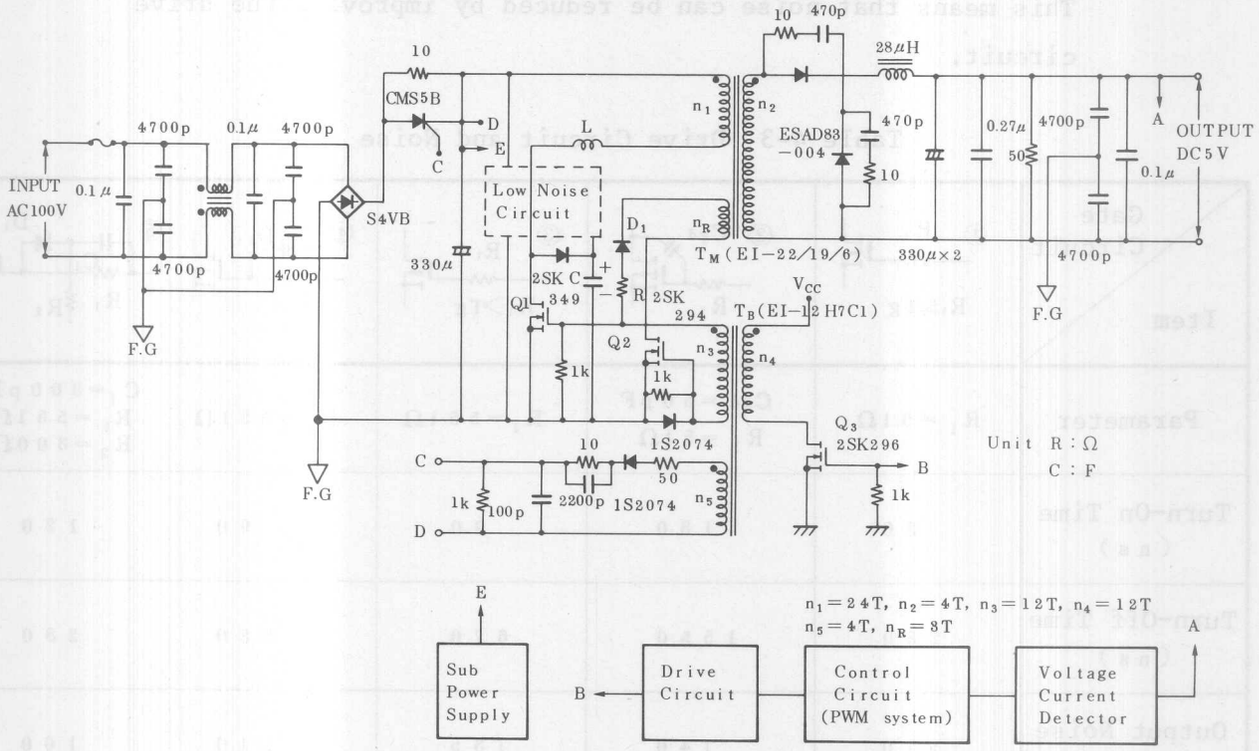


Fig. 4-27 Block Diagram of One-Transistor Forward System, 500 kHz, 50W (5V, 10A).

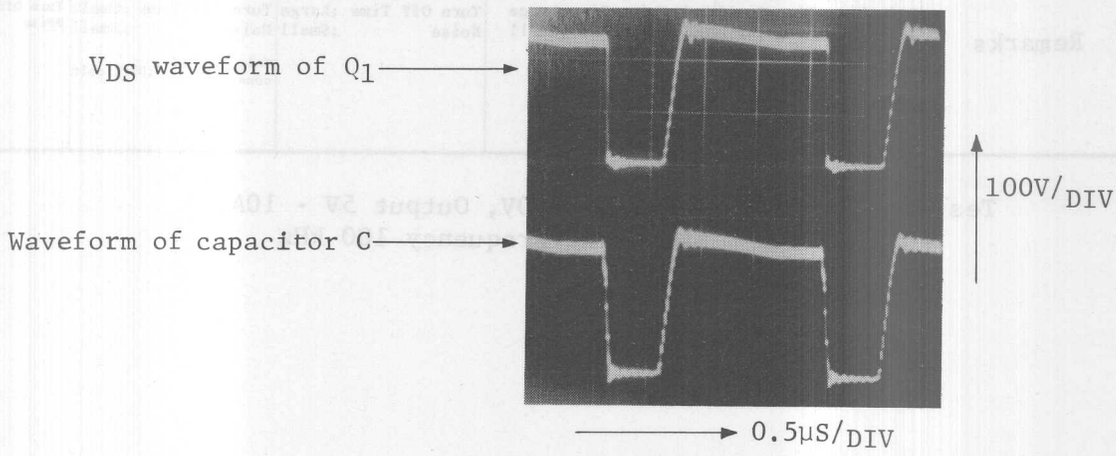


Fig. 4-28 Waveforms (at 5V, 9.1A)

[High speed drive circuit]

To allow a higher frequency switching power, the most important thing is to turn off the main switching device in high speed. A control current with a high peak value is necessary to turn a power MOS FET off. Here, we adopt a simple circuit by utilizing the main circuit to supply a high peak current at turn-off. This circuit operates as follows.

When the MOS FET Q_3 turns on, a current flows via transformer T_B to Q_1 gate, and Q_1 is turned on. In consequence, a voltage is induced in the coils n_1 and n_R. The black dot in the figure indicates the positive polarity. Q_2 is off with inverse bias by voltage drop in the diode D_2.

Next, when Q_3 is turned off, the current in T_B flows through the gate to source of Q_1 and the source to gate of Q_2 and turns Q_2 on. Q_1 is still on, right after Q_2 turns on.

Therefore, the above mentioned voltage in the coils n_1 and n_R still remains. By Q_2 turning on, current from n_R flows to the source - gate of Q_2 and Q_1, the resistor R, and the diode D_1 and turns Q_1 off. When Q_1 turns off, a reverse voltage to the dotted polarity is generated in n_1 and n_R. This voltage is blocked by D_1.

With the above operation, an inverted high peak gate current can be generated from the main circuit to Q_1.

[Noise reduction]

The output noise is reduced by L and C in the circuit. This controls the voltage change rate by time of which voltage is supplied to the primary coil at on or off of the main switching device. The reactor L restrains the current increase in the primary coil n_1, when Q_1 (main switching device) turns on. The capacitor C restrains the change rate of the voltage induced in the primary coil n_1, when Q_1 turns off.

The part encircled by a dotted line in the figure is discharge circuit for the capacitor C which is charged with the polarity indicated in the figure after Q_1 was turned off.

This discharge circuit feeds the charged energy in C back to the rectified DC supply in the primary part, while Q_1 is on. The circuit also discharges C to 0V until Q_1 is turned off. The constants of L and C are determined by analyzing the harmonics in the voltage supplied to the

primary coil n_1, so that the resonant frequency of the equivalent high-pass filter between primary and secondary coils is removed.

The output noise waveform from the above described circuit, and without countermeasures, are shown in Fig. 4-29 and Fig. 4-30 respectively. You can see in the figures that the output noise is significantly reduced.

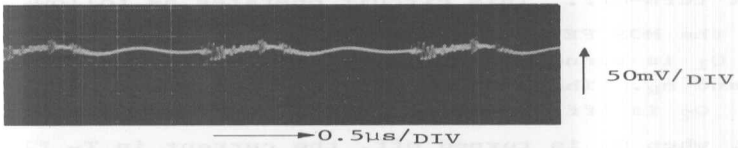


Fig. 4-29 Output Noise Waveform with the Circuit Introduced (Synchroscope 150 MHz, 5V, 10A)

Fig. 4-30 Output Noise Waveform without Countermeasures (Synchroscope 150 MHz, 5V, 10A)

A comparison of the volume with main transformer, choke coil and output smoothing capacitor in 50 kHz, 50W (5V, 10A) output switching power supply made on an experimental basis in our company is shown in Table 4-4. In 500 kHz switching power supply, 26% of the main transformer volume, 25% of the choke coil volume and 50% of the output smoothing capacitor volume; i.e. 65% of the total volume were reduced, in comparison with 50 kHz switching power supply.

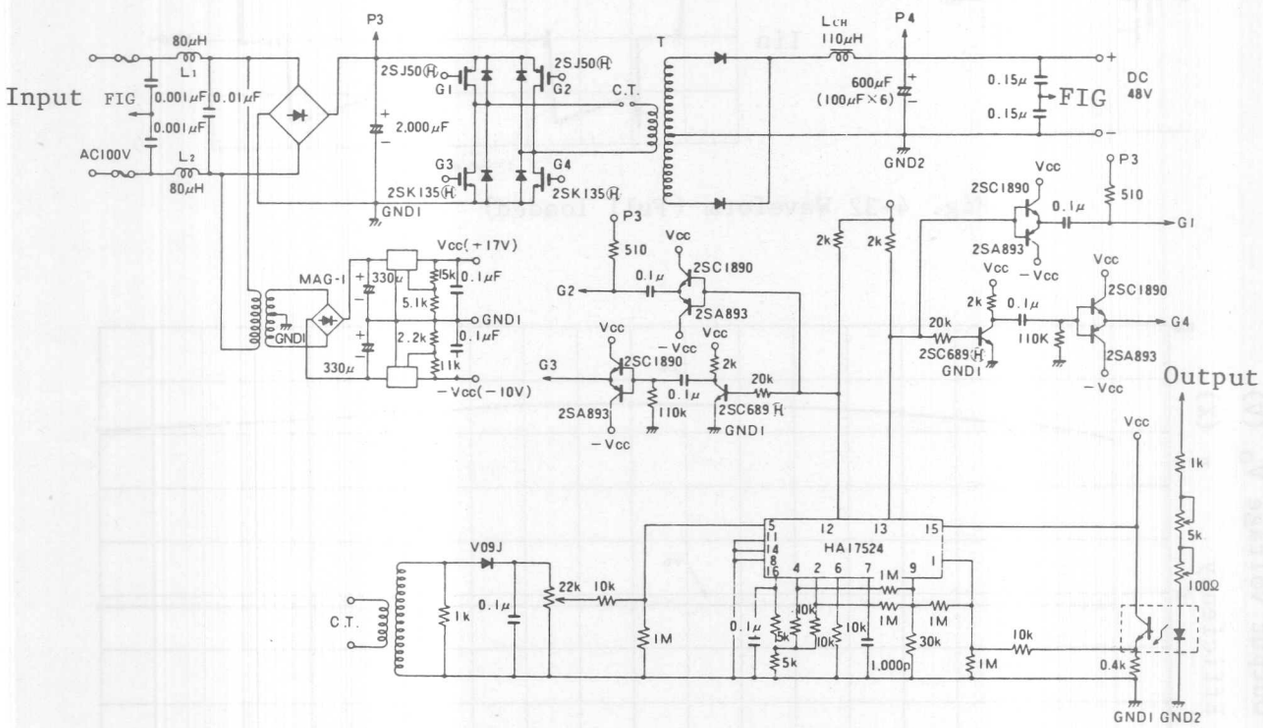
Fig. 4-4 A Comparison of the Volume of Main Transformer, Choke Coil and Output Smoothing Capacitor in 5V, 10A Output Switching Power Supplys

	50kHz switching power supply	500kHz switching power supply
Main transformer volume	16000mm^3	4200mm^3 (26%)
Choke coil volume	8500mm^3	2100mm^3 (24%)
Output smoothing capacitor volume	16000mm^3	8000mm^3 (50%)

● Four-transistor full-bridge type 100kHz, 400W switching regulator

Fig. 4-31 shows the circuit of four-transistor full-bridge type switching regulator. This circuit has the following characteristics.

- output; 400W (48V, 8A)
- input; AC 100V
- operation frequency; 100kHz
- control IC; HA17524
- isolation; photo coupler
- efficienty; at full load 80%
  ; at 200W output 85%



L_1,L_2:T type core φ1.5mm wire 13T
LCH:EI50 core Cap 0.3mm
φ1mm wire 6 wires wound separately

T:EI60 core
1st side φ1.5mm Wire 7T
2nd side φ1mm wire 4T;
5 wires wound separately

C.T.:EI30 core
1st side φ1.5mm wire 1T
2nd side φ0.5mm wire 25T

Fig. 4-31 Four-transistor Full Bridge System Switching Regulator

4.APPLICATION HINTS

This circuit operates as a switching regulator (AC 100V, direct rectification type), using N-channel & P-channel MOS FET's for four-transistor full bridge. To make good use of the high speed capability of power MOS FETs, the switching cycle is set at 100kHz. As a result, we had 80% efficiency at full load and maximum 85% efficienty (at 200W output).

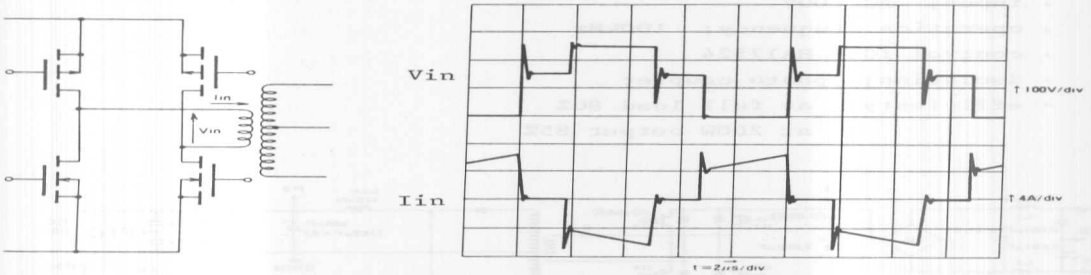


Fig. 4-32 Waveform (Full loaded)

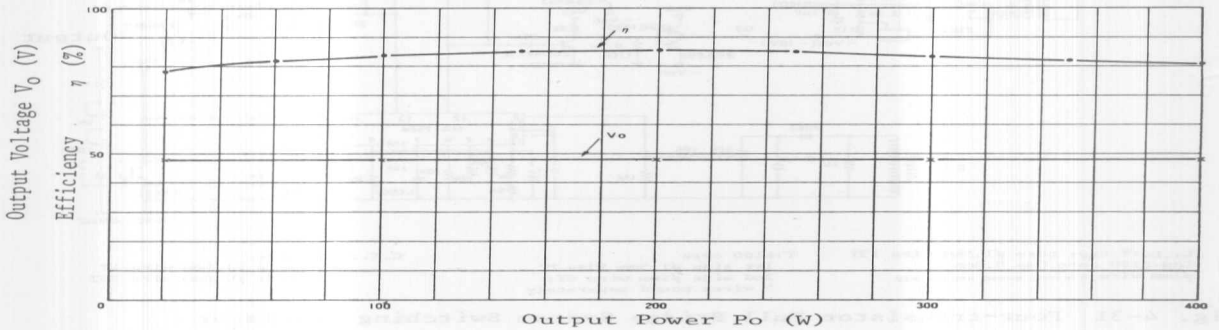


Fig. 4-33 Output Voltage and Efficiency vs. Output Power Characteristics

● One-transistor system 250kHz, 60W, low noise switching regulator

Fig. 4-34 shows the circuit of one-transistor system switching regulator. It has the following characteristics.

- output; 5V, 12A
- input; 48±5V
- operation frequency; 250kHz
- efficiency; at full load 83%
  ; at 20W output 87%
- spike noise voltage; $10mV_{p-p}$

The noise reduction method used in this circuit is as follows:

(1) Good use is made of the source connected case of the power MOS FET.

(2) Loose coupling of the output transformer.

(3) Switching curve softened by mirror integration with the primary circuit of transformer, connecting the capacitor between drain and source.

With the above method, the spike components will be removed almost completely. Radiation to the outside can be prevented by shielding.

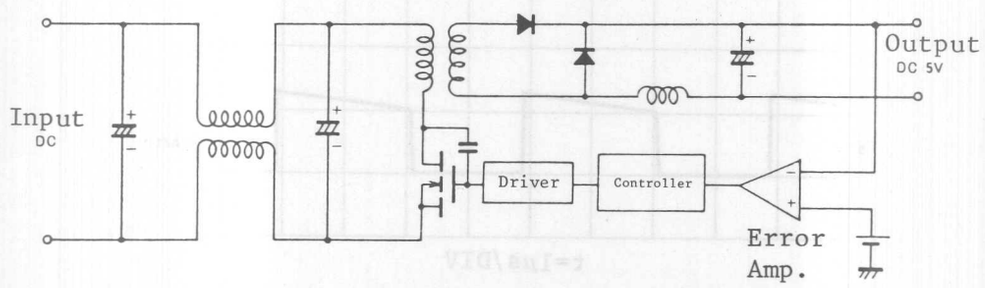


Fig. 4-34 One-transistor type Switching Regulator (Block Diagram)

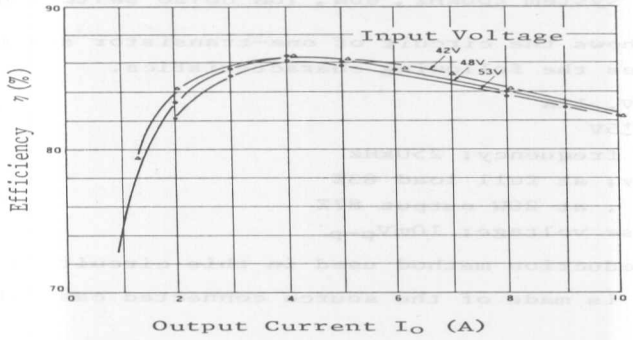


Fig. 4-35 Efficiency vs. Output Current Characteristics

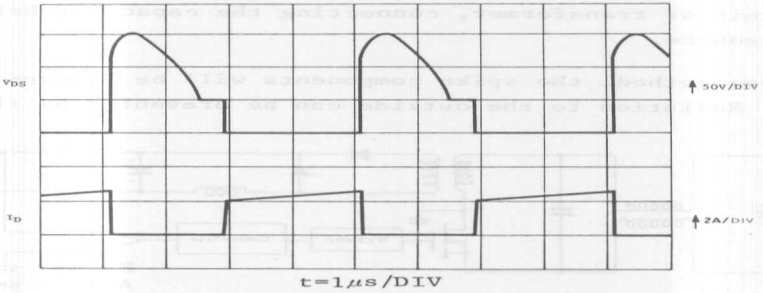


Fig. 4-36 Waveform

4.2.2 High-speed Drive Circuit

A switching regulator has two types of drive circuits; one is direct type drive and the other is isolated type drive.

● Direct type

(1) Additional Buffer Circuit

Fig. 4-37 shows additional buffer Circuit. In this circuit, the output impedance of the drive circuit is lowered through NPN and PNP complementary symmetry emitter follower, resulting in high speed.

(2) Positive Feedback type Circuit

Fig. 4-38 shows positive feedback type circuit, in which positive feedback is applied by sub-coil (n_3), resulting in high speed switching. The operation theory is as follows.

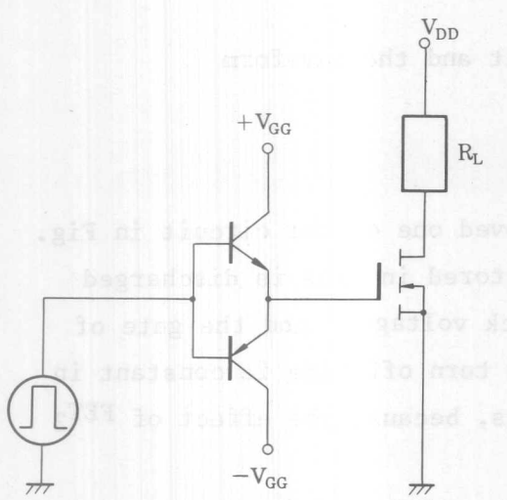
i) FET_1 is driven by inverter and drain current flows.

ii) Voltage is generated by n_3 and the input capacitance (Ciss) is charged through R_1.

iii) According to turn ON process of FET_1, a positive feedback is applied to the gate.

iv) When the FET_2 turns ON and the gate of FET_1 is grounded, resulting in discharge of Ciss, the FET_1 turns OFF.

Fig. 4-39 shows the waveform between drain and source.



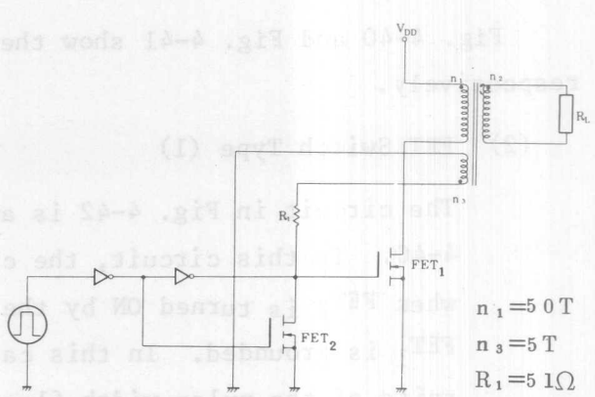


Fig. 4-37 Additional Buffer Circuit Fig. 4-38 Positive Feedback Circuit

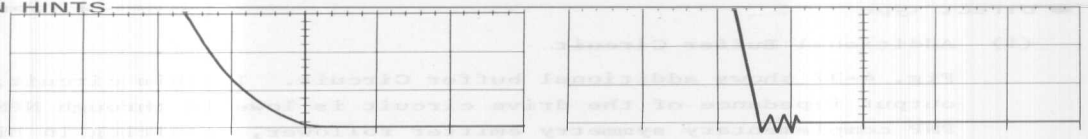


Fig. 4-39 Drain-Source Waveform($I_D = 2$ A) (2SK298)
$n_1 = 50$ T , $n_3 = 5$T , $R_1 = 51\Omega$

● Isolation Type

The following circuits operate by making use of the flyback voltage which is generated during the OFF period.

(1) Diode Switch Type

This circuit is the simplest. In this circuit, the input capacitance of FET_1 is forced to be discharged by the flyback voltage which is generated when FET_2 turns OFF, and high speed switching is achieved. This circuit has a problem in that the turn off time of FET_1 is not constant because the flyback energy depends on the ON time (pulse width).

Fig. 4-40 and Fig. 4-41 show the circuit and the waveform respectively.

(2) FET Switch Type (1)

The circuit in Fig. 4-42 is an improved one of the circuit in Fig. 4-40. In this circuit, the charge stored in Ciss is discharged when FET_2 is turned ON by the flyback voltage, and the gate of FET_1 is grounded. In this case, the turn off time is constant in spite of the pulse width fluctuations, because the effect of FET_2 is larger than that of the flyback.

Fig. 4-43 shows the waveform between drain and source.

(3) FET Switch Type (2)

The circuit shown in Fig. 4-44 yields even higher performance than that of Fig. 4-42. In this circuit, when FET_2 is turned ON by the flyback voltage, the voltage generated at n_5 will discharge the FET's Ciss positively with the time constant R·Ciss. As obvious from the operation waveform of Fig. 4-45, the turn on time and the turn off time are both less than 30ns.

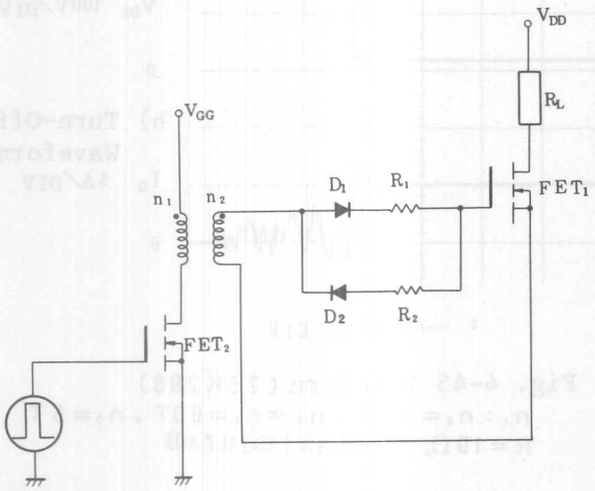


Fig. 4-40 Diode Switch Type

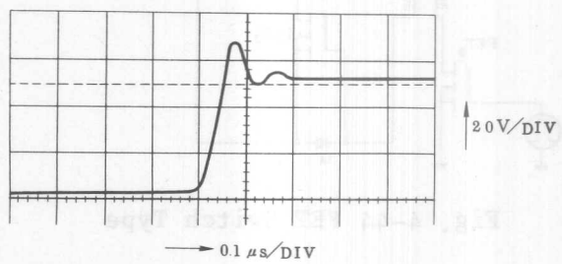


Fig. 4-41 Drain-Source Waveform (I_D = 2A, 2SK 298)
$n_1 : n_2 = 1 : 1$
$R_1 = R_2 = 50\Omega$

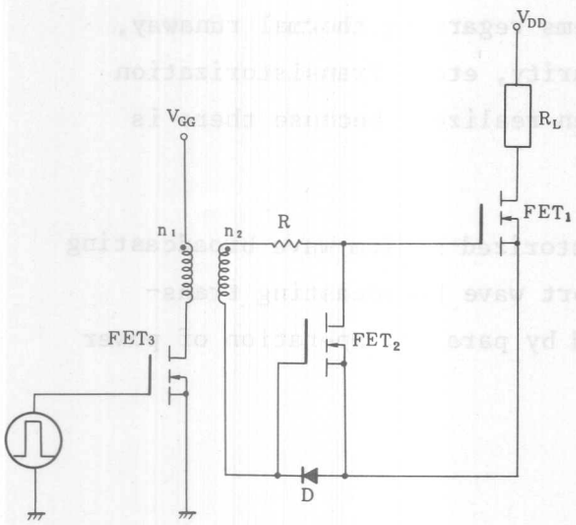


Fig. 4-42 FET Switch Type

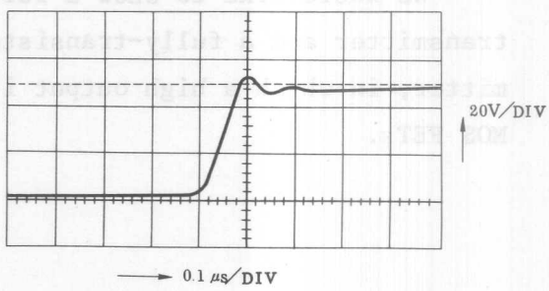


Fig. 4-43 Drain-Source Waveform
(I_D = 2A, 2SK 298)
$n_1 : n_2 = 1:1$ $R = 50\Omega$

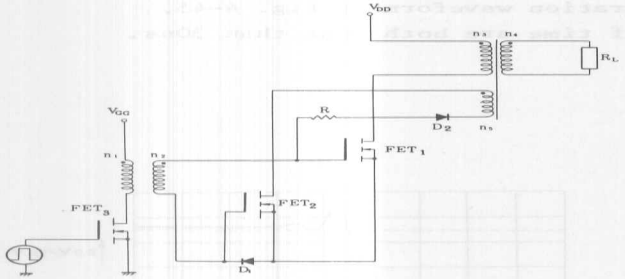


Fig. 4-44 FET Switch Type

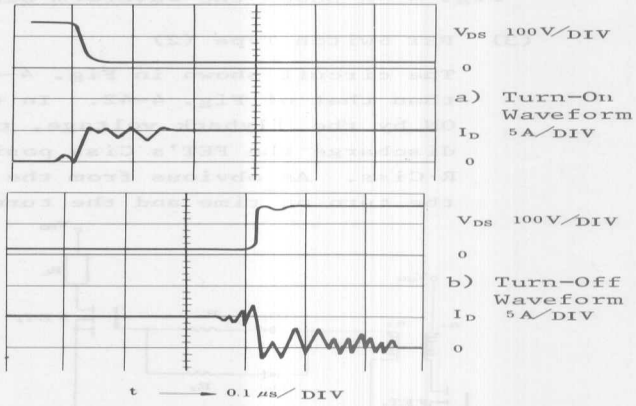


Fig. 4-45 Waveform (2SK298)
$n_1 : n_2 = 1 : 1$, $n_3 = n_4 = 60T$, $n_5 = 6T$
$R = 10\Omega$, D_1, D_2 : 1S2074Ⓗ

4.3 High Frequency Power Amplifier

As for transmitter applications, transistorization of 5 ∼ 10kW medium wave broadcasting transmitters has been achieved. The bipolar transistors used however, have some problems regarding thermal runaway, frequency characteristic, modulation linearity, etc. Transistorization in short wave broadcasting has not yet been realized, because there is not a suitable device.

We would like to show a fully-transistorized medium wave broadcasting transmitter and a fully-transistorized short wave broadcasting transmitter, in which a high output is provided by parallel operation of power MOS FETs.

4.3.1 1kW Medium Wave Broadcasting Transmitter *1)

Fig. 4-46 shows a block diagram of a 1kW medium wave broadcasting transmitter. This system has the following characteristics.

- Frequency; 1197kHz
- Output; 1100W
- Power supply; AC 200V, Single phase 50Hz
- Efficiency (without modulation)
  - Total efficiency; 61.9%
  - Efficiency at modulation part; 93.6%
  - Efficiency at non-modulation part; 84.4%
- Modulation System; pulse width modulation

Power MOS FETs used in the transmitter provide the following features.

(1) Low Power Consumption

Power MOS FET requires no pre-modulation because of its high efficiency and high gain.

(2) High Performance

The distortion introduced by the pulse width modulation stage is very small because of its switching speed. A high carrier frequency can be used in the PWM modulator for extended overall frequency response.

(3) High Reliability

The power MOS FET is inherently rugged and may be connected in parallel without any special considerations. It is possible to use many devices in parallel, and through their redundancy, high reliability is realized.

(4) Easy Thermal Design

The use on many parallel devices aids thermal dispersion, and results in easy thermal design.

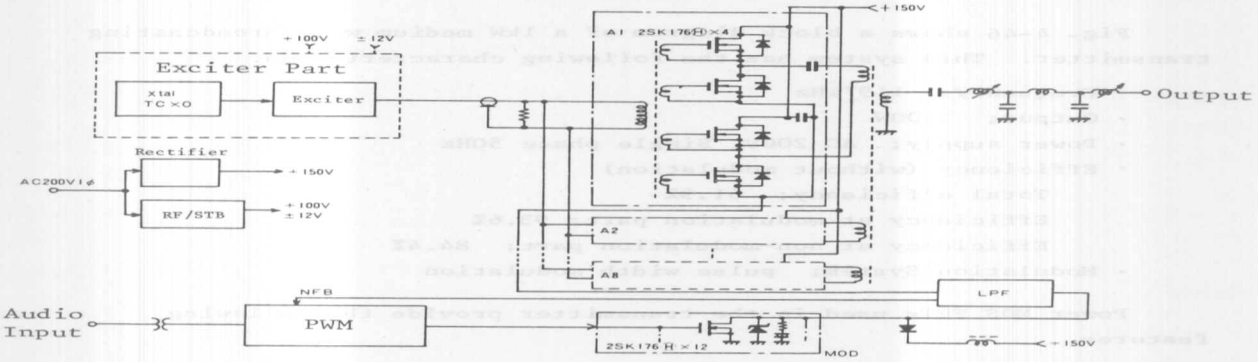


Fig. 4-46 Block Diagram of 1kW Medium Wave Broadcasting Transmitter

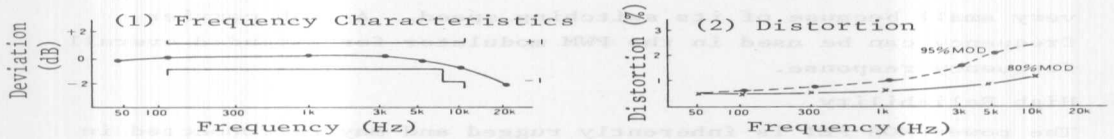


Fig. 4-47 Main Characteristics

4.3.2 600W Short Wave Broadcasting Transmitter *2)

Fig. 4-48 shows the circuit of the power amplifier circuit. The characteristics of this circuit are as follows:

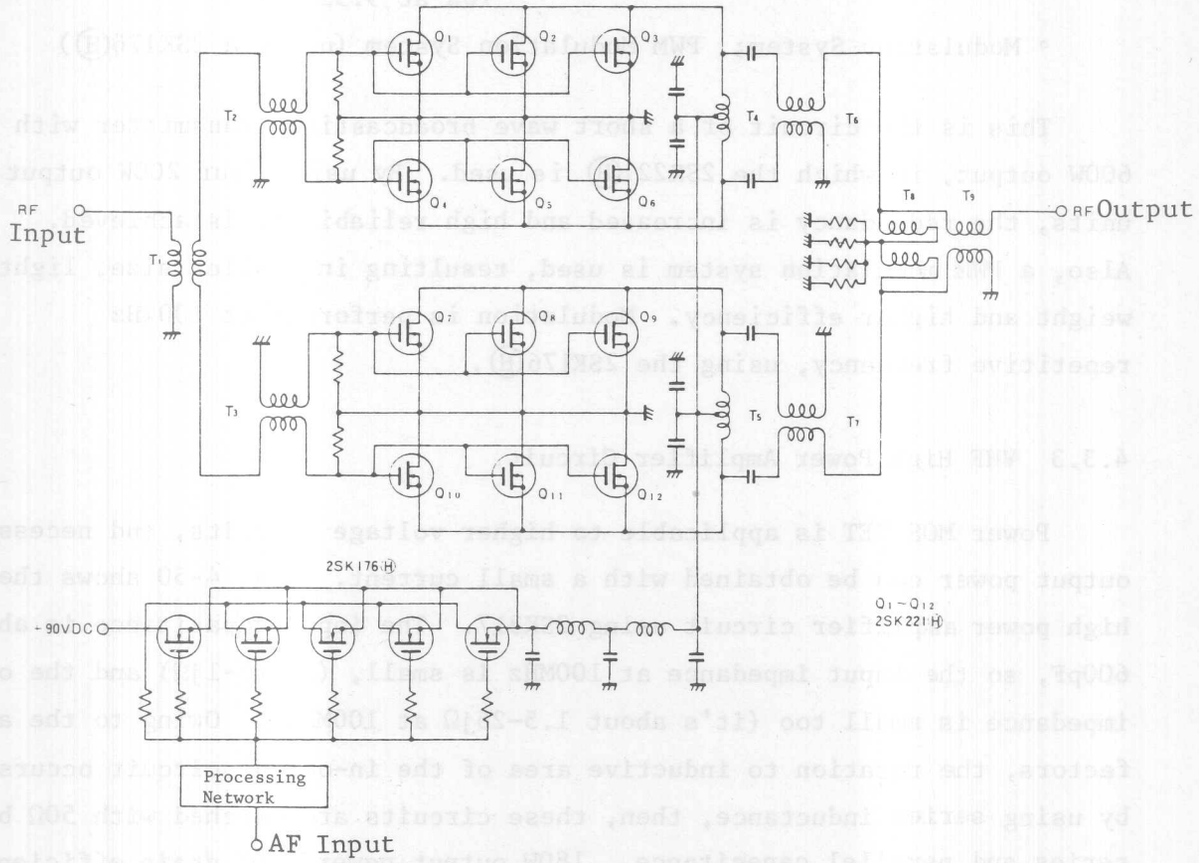
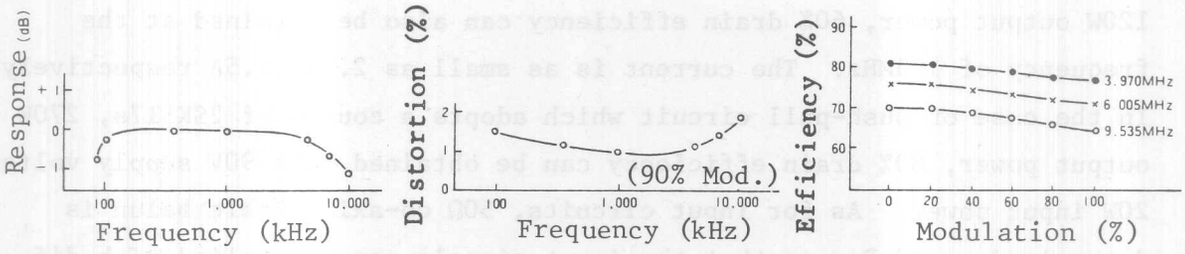


Fig. 4-48 Power Amplifier (200W Unit)



(1) Frequency Characteristics (2) Distortion Characteristics (3) Power Efficiency

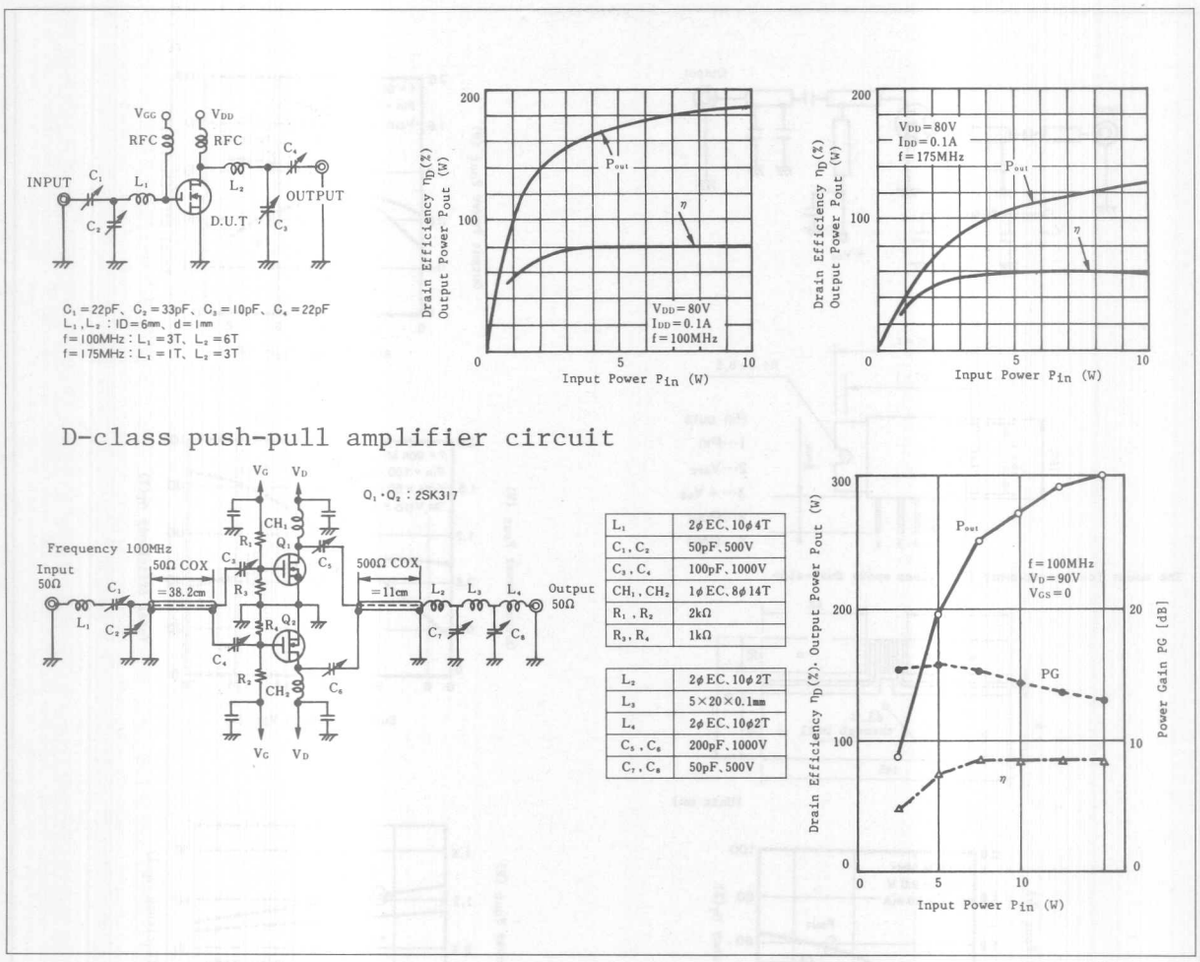
Fig. 4-49 Main Characteristics

- Frequency; 3.970MHz, 6.005MHz, 9.53MHz
- Output; 600W (four 200W units using 2SK221Ⓗs)
- Efficiency (without modulation); 81% at 3.970MHz
  77% at 6.005MHz
  70% at 9.535MHz
- Modulation System; PWM Modulation System (using a 2SK176Ⓗ)

This is the circuit of a short wave broadcasting transmitter with 600W output, in which the 2SK221Ⓗ is used. By using four 200W output units, the redundancy is increased and high reliability is achieved. Also, a PWM modulation system is used, resulting in smaller size, lighter weight and higher efficiency. Modulation is performed at 100kHz repetitive frequency, using the 2SK176Ⓗ.

4.3.3 VHF High Power Amplifier Circuit.

Power MOS FET is applicable to higher voltage circuits, and necessary output power can be obtained with a small current. Fig. 4-50 shows the VHF high power amplifier circuit using 2SK317. The input capacitance is about 600pF, so the input impedance at 100MHz is small, (Z_{in}=1-1jΩ) and the output impedance is small too (it's about 1.5-25jΩ at 100MHz). Owing to the above factors, the rotation to inductive area of the in-output circuit occurs by using series inductance, then, these circuits are matched with 50Ω by series and parallel capacitance. 180W output power, 80% drain efficiency can be obtained with 80V supply voltage, 8W input power, 100MHz frequency. 120W output power, 60% drain efficiency can also be obtained at the frequency of 175MHz. The current is as small as 2.8A, 2.5A respectively. In the case of push-pull circuit which adopts a couple of 2SK317s, 270W output power, 80% drain efficiency can be obtained with 90V supply voltage, 20W input power. As for input circuits, 50Ω co-axial cable balun is determined as 38.2cm so that the input signals can be applied with different phases. The output circuit consists of balun and filter, and the length of the output balun is determined as 11cm, aiming at maximum efficiency.



L_1	2φEC, 10φ4T
C_1, C_2	50pF, 500V
C_3, C_4	100pF, 1000V
CH_1, CH_2	1φEC, 8φ14T
R_1, R_2	2kΩ
R_3, R_4	1kΩ

L_2	2φEC, 10φ2T
L_3	5×20×0.1mm
L_4	2φEC, 10φ2T
C_5, C_6	200pF, 1000V
C_7, C_8	50pF, 500V

Fig. 4-50 VHF High Power Amplifier Circuit

(1) 900MHz 1W power amplifier circuit (PF0001)

The PF0001 is a high frequency power MOS FET amplifier and the output power; 1W (typ.) can be obtained. It is single stage amplifier using the HS8709 chip. Fig. 4-51 shows the internal equivalent circuit and dimensional outline of the PF0001. The matching circuit is formed on the ceramic substrate by using micro-strip line and chip condenser. 1.1W output power, 50% total efficiency, power gain 10dB (typ.) can be obtained at 100mW input power. As for gain reduction value controlled variable by the APC terminal, 5dB or more can be obtained by changing the APC voltage from 8V to 0V.

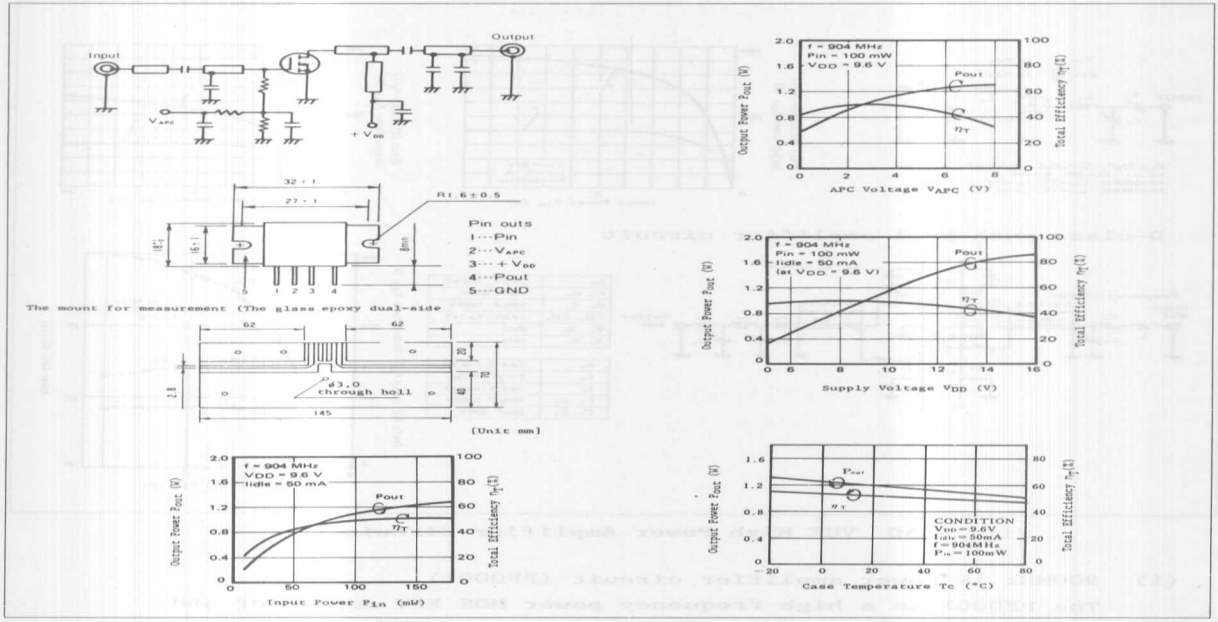


Fig. 4-51 900MHz 1W Power Amplifier Circuit (PF0001)

(2) 900MHz 8W power amplifier circuit (PF0002)

The PF0002 is a high frequency power MOS FET amplifier. It is a two stage amplifier using HS8709 and HS8711 chips. Fig. 4-52 shows the internal equivalent circuit and dimensional outline. The applicable range of supply voltage is 7 to 16V, the frequency range is 860 to 910MHz. As for gain reduction value controlled variable by the APC terminal, 5dB or more can be obtained by changing the APC voltage 8V to 0V.

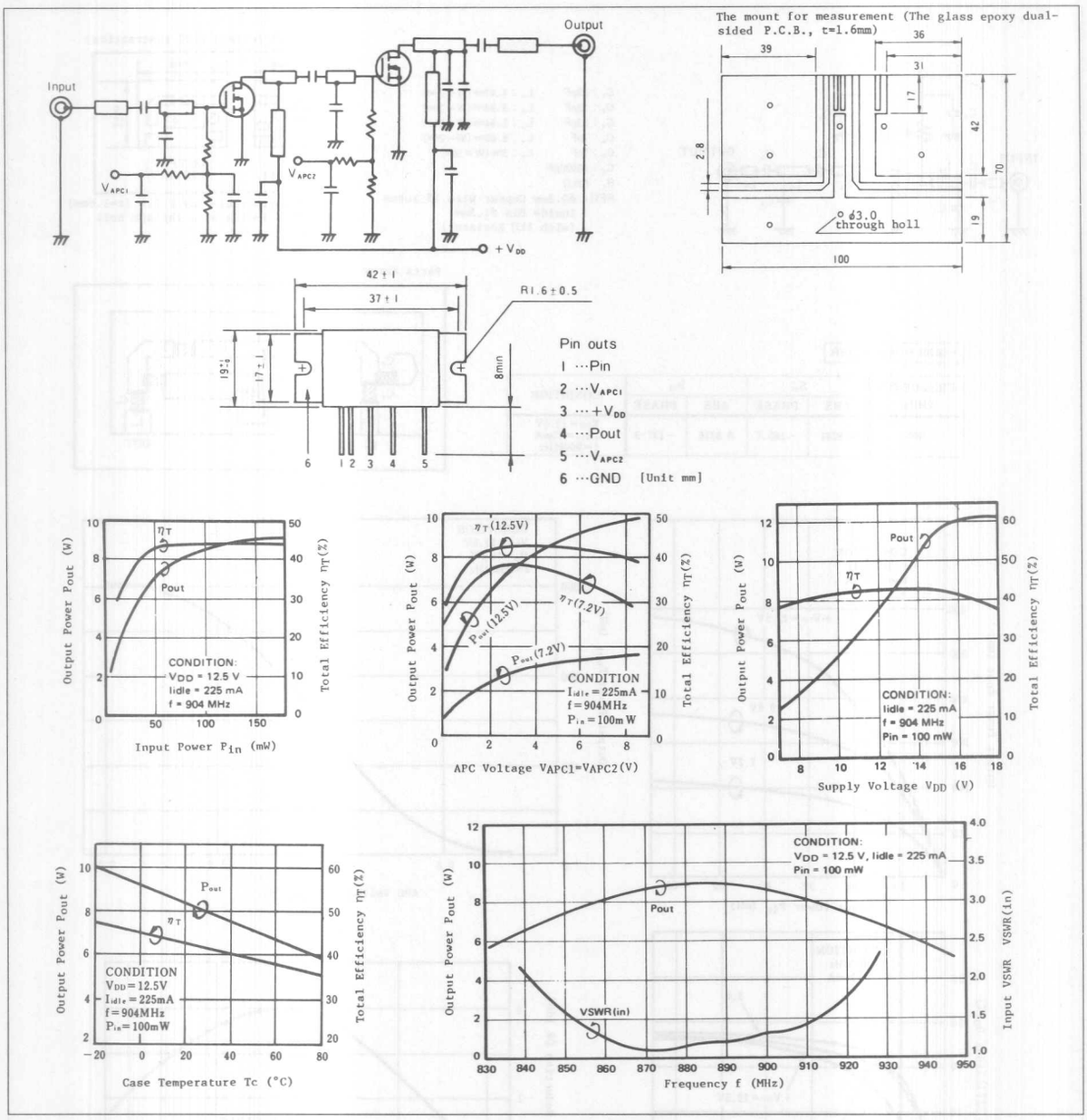


Fig. 4-52 900MHz 8W Power Amplifier Circuit (PF0002)

(3) 900MHz power amplifier circuit (HS8708)

The HS8708 is power MOS FET and its applicable input power is 10 to 50mW. It is sealed into the chip carrier. Fig. 4-53 shows the 900MHz pre-drive circuit using this FET. 400mW output power, 40% efficiency can be obtained at 20mW input power, when V_{DD}=12.5V. The output power can be controlled from 300mW up to almost 0mW by changing the gate voltage from 2.0V to 0.

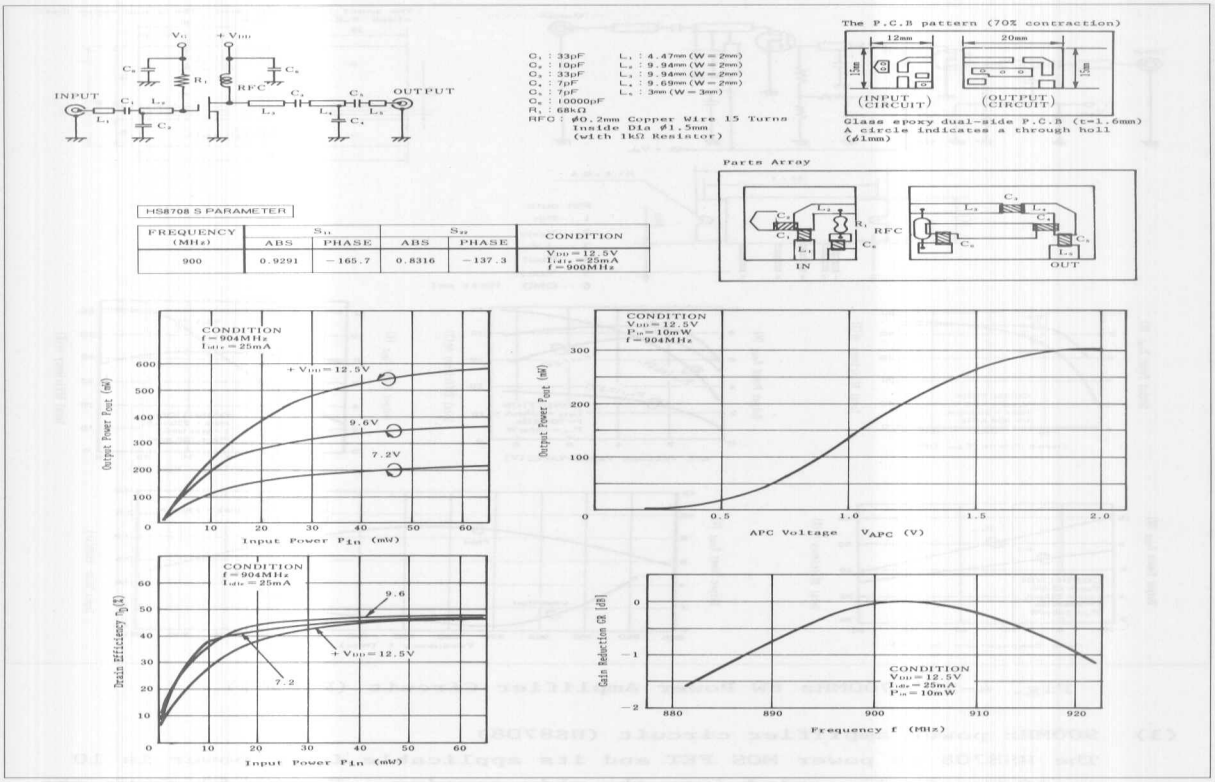


Fig. 4-53 900MHz Power Amplifier Circuit (HS8708)

(4) 900MHz power amplifier circuit (HS8709)

The HS8709 is power MOS FET of 100mW input power. The chip used for the PF0001 and the drive stage of PF0002, is sealed into the chip carrier. Fig. 4-54 shows the drive circuit by using this FET. The output power 1.5W, 50% efficiency can be obtained when V_{DD}=12.5V, 100mW input power.

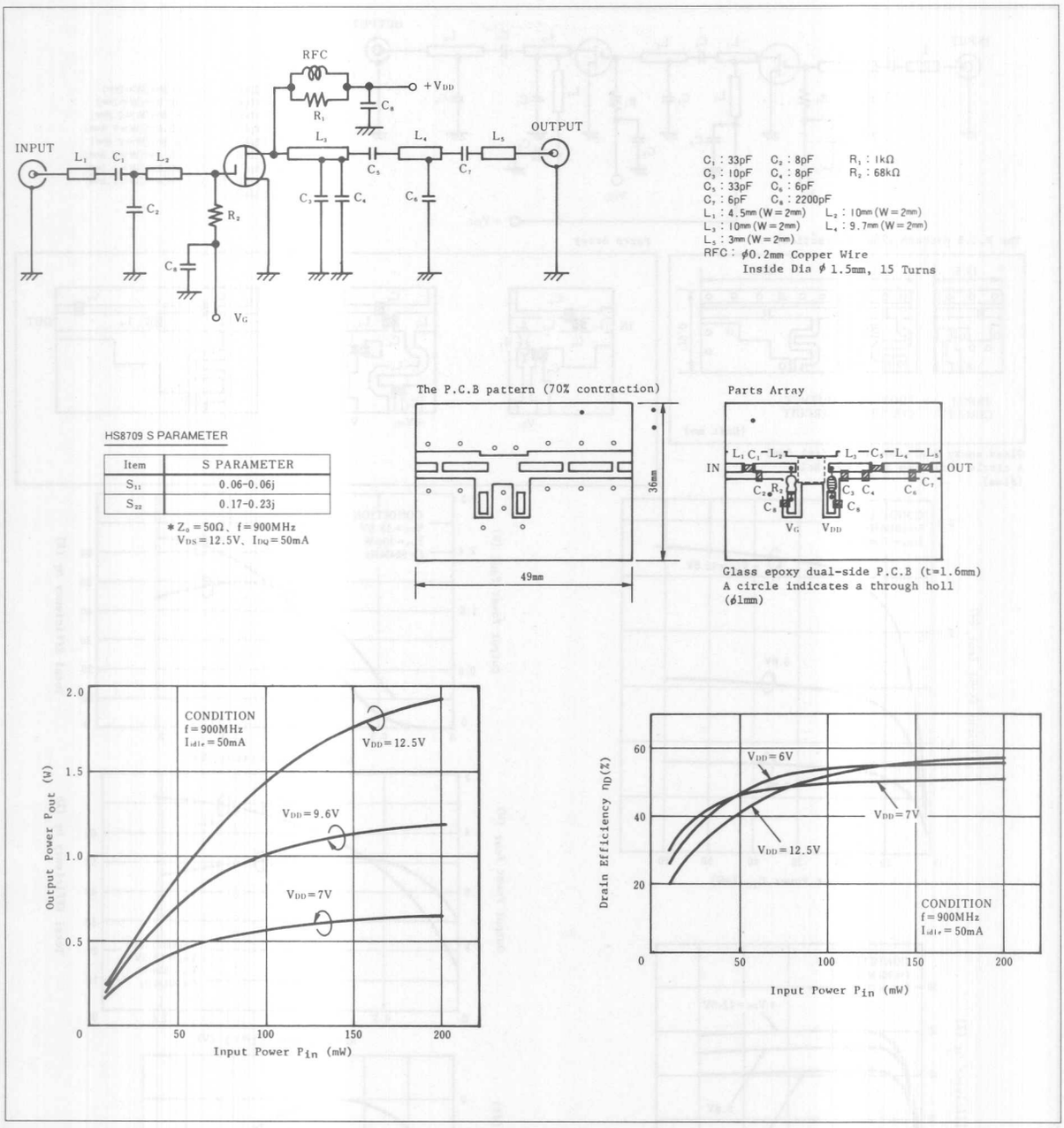


Fig. 4-54 900MHz Power Amplifier Circuit (HS8709)

(5) 900MHz two stage power amplifier circuit

Fig. 4-55 shows a two stage power amplifier circuit using HS8708, HS8709. 2.5W output power, 50% total efficiency can be obtained when V_{DD}=12.5V, 20mW input power. The power control by using 1st and 2nd gate voltages in the case of 10mW input power, the output power can be controlled from 2.5W to almost 0, by changing the gate voltage from 2V to 0. The gain reduction value is about 7dB with 30mW input power.

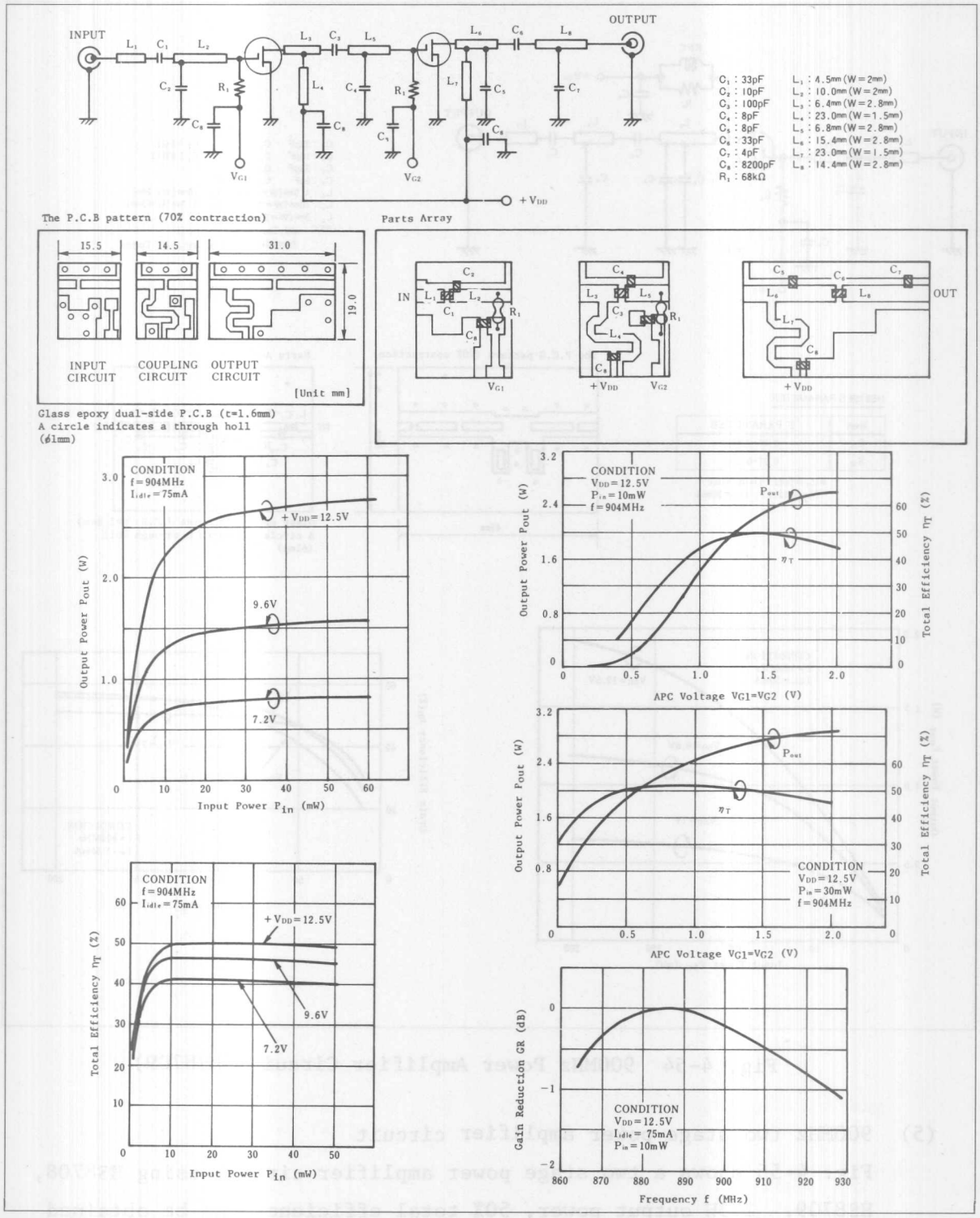


Fig. 4-55 900MHz Two Stage Power Amplifier Circuit

(6) 900MHz power amplifier circuit (HS8711)

The HS8711 is power MOS FET used for final stage of PF0002. Fig. 4-56 shows the power amplifier circuit using this FET. 8W output power, 55% efficiency can be obtained when V_{DD}=12.5V, 1.6W input power. In the case of 7V supply voltage, 3.5W output power, 49% efficiency can also be obtained.

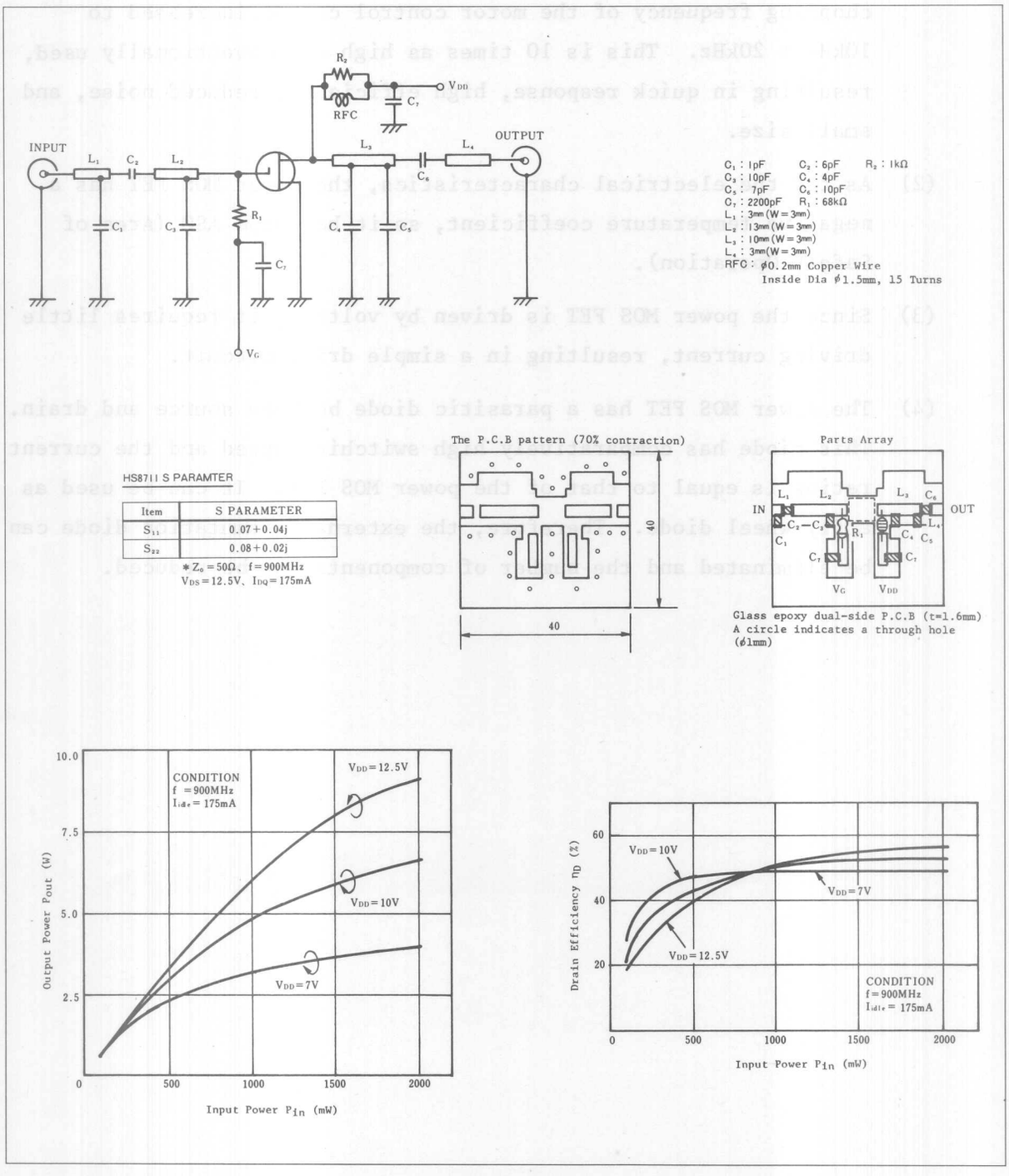


Fig. 4-56 900MHz Power Amplifier Circuit (HS8711)

4.4 Motor Control

Formerly, bipolar transistors or thyristors have been used for speed control of DC and AC motors. Recently, however, power MOS FETs are used for motor control, owing to their low R_{ON}. Power MOS FETs used for motor control have the following features.

(1) Since the switching speed of the power MOS FET is very fast, the chopping frequency of the motor control can be increased to 10kHz ∿ 20kHz. This is 10 times as high as conventionally used, resulting in quick response, high efficiency, reduced noise, and small size.

(2) As for the electrical characteristics, the power MOS FET has a negative temperature coefficient, so it has wide ASO (Area of Safety Operation).

(3) Since the power MOS FET is driven by voltage, it requires little driving current, resulting in a simple drive circuit.

(4) The power MOS FET has a parasitic diode between source and drain. This diode has comparatively high switching speed and the current rating is equal to that of the power MOS FET. It can be used as a fly-wheel diode. Therefore, the external commutation diode can be eliminated and the number of components can be reduced.

Table 4-4 The Characteristics of Power MOS FET and Advantages in Motor Control

Features	Advantages in motor control
Switching speed is fast.	High efficiency, reduced noise and small-sized by high operating frequency
Voltage control	Little driving power, resulting in a simple drive circuit
Negative temperature coefficient of current	Easy to have higher current capability with parallel connection due to no local current concentration
Built-in diode between drain and source	It can be used as a fly-wheel diode, and the number of components can be reduced
P/N channel complimentary	The number of components can be reduced by the simple drive circuit

Fig. 4-57 shows inverter circuit in which 2SK313 is used at $Q_1 \sim Q_6$. The built-in diode between drain and source is relatively high speed and can be used as a fly-wheel diode. Therefore, external high-speed fly-wheel diode is not required, the number of components can be reduced. As for electrically short accident in the inverter circuit, Power MOS FETs take longer time than bipolar transistor to breakdown, and over-current protection circuits can be easily designed. Fig. 4-58 shows the results of load short test.

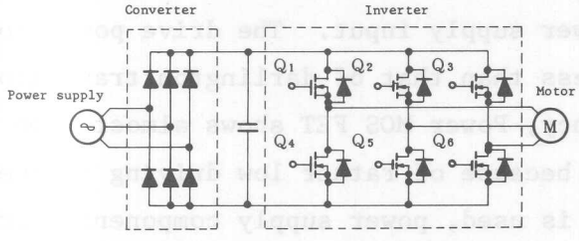


Fig. 4-57 Power MOS FET Inverter

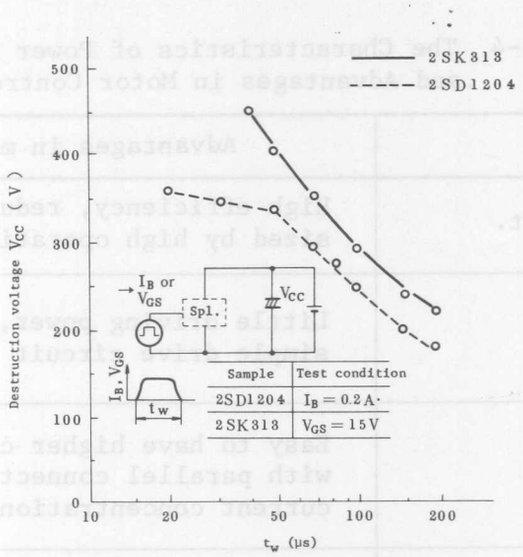


Fig. 4-58 Destruction voltage at load short test

● Gate Drive Circuit

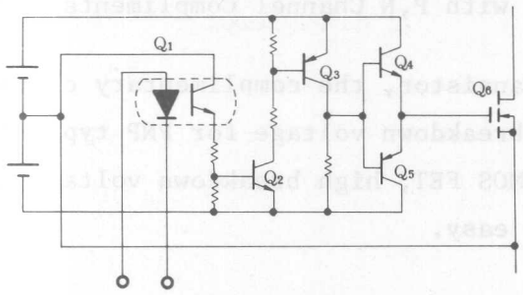
Fig. 4-59 shows basic gate drive circuit in which Power MOS FET is used. There are several kinds of circuit. The circuit needs less drive power due to voltage control than the current control of bipolar transistor, and can compose by small signal transistors.

The comparison of driving power with bipolar transistor is shown in Fig. 4-60.

This figure shows the characteristics of 1.2kW DC brushless motor drive using the inverter circuit in which power MOS FET, 2SK313 (V_{DSS} 450V, I_D 12A) or darlington transistor 2SD1204 (V_{CEO} 400V, I_C 15A) is used. As for driving power, the total of the transformer loss at driving circuit and the control circuit loss and the drive circuit loss is measured as sub power supply input. The drive power loss of Power MOS FET, 2SK313, is less than that of darlington transistor. Concerning with inverter efficiency, Power MOS FET shows almost same level as darlington transistor because of rather low driving frequency of 2.2kHz.

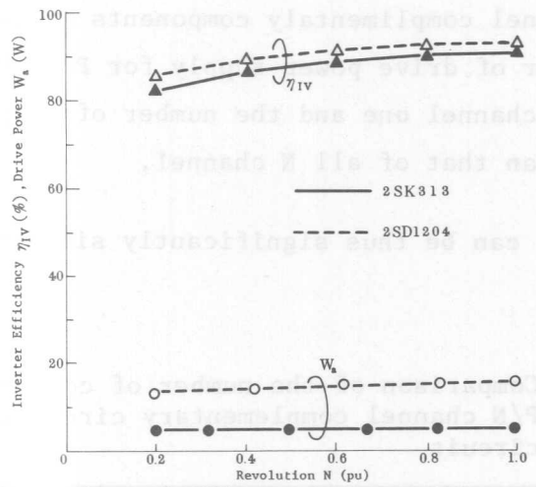
If Power MOS FET is used, power supply components for driving can be simplified due to low drive power loss (Fig. 4-61). Fig. 4-61 (a) shows the method that obtains positive and negative power supply from inverter input DC voltage using zener diode. Fig. (b) shows the method that obtains positive and negative power supply using power supply transformer. The method using power supply transformer does not need power stability due to voltage control gate drive.

The gate drive circuit can save energy and be minimize by using Power MOS FET.



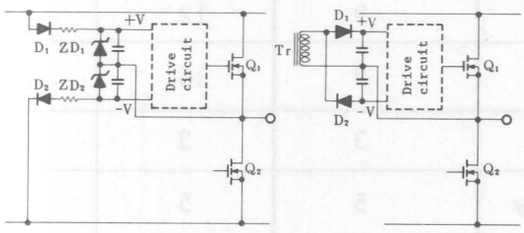
Q_1; Photo Coupler
Q_2~Q_5; Drive Transistor
Q_6; Power MOS FET

Fig. 4-59 Gate Drive Circuit of Power MOS FET



Note: 1 pu=6,000rpm Torque 20kg·cm

Fig. 4-60 Comparison of Drive Power of 1.2 kW DC Brushless Motor Operation



Q_1, Q_2; Power MOS FET
D_1, D_2; Diode
ZD_1, ZD_2; Zener Diode
Tr ; Power Supply Transformer

Fig. 4-61 Structure of Drive Power Supply for Power MOS FET on Upside Arm

● Gate Drive Circuit with P,N Channel Complimentary Power MOS FET

As for bipolar transistor, the complimentary characteristics of current gain and high breakdown voltage for PNP type is difficult to design. As for Power MOS FET, high breakdown voltage and high current of P channel is rather easy.

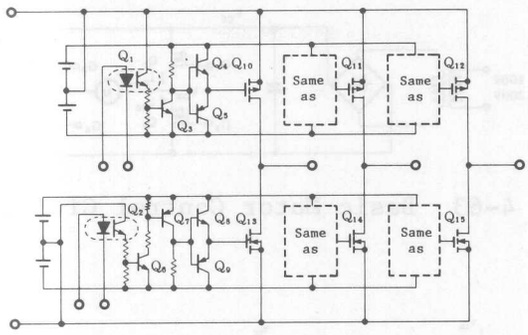
The circuit with P and N channel complimentary Power MOS FET is shown in Fig. 4-62. If P channel devices are used in upside arm of inverter and N channel devices are in the under arm, drive power supply are needed only for each arm. Table 4-5 shows comparison between P/N channel and all N channel complimentaly components about the number of components. The number of drive power supply for P/N channel is as half as that of all N channel one and the number of components for P/N channel is 24% less than that of all N channel.

The drive circuit can be thus significantly simplified.

Table 4-5 Comparison of the number of components between P/N channel complementary circuit, all N channel circuit

	P/N Channel Complementary Circuit		All N Channel Circuit	
	Upside Arm	Under Arm	Upside Arm	Under Arm
Transistor	9	12	12	12
Resistor	9	15	15	15
Photo Coupler	3	3	3	3
Drive Power Supply	5	5	15	5
Total	26	35	45	35
	61		80	

Note; Unit (piece)



Q_1 , Q_2 ; Photo Coupler
Q_3 ~ Q_9 ; Drive Transistor
Q_{10} ~ Q_{12} ; P Channel Power MOS FET (2SJ116)
Q_{13} ~ Q_{15} ; N Channel Power MOS FET (2SK313)

Fig. 4-62 Drive Circuit with P and N Channel Complementary Power MOS FET

4.4.1 Precautions in Handling the Built-in Diode

An built-in diode of the power MOS FET is used as a commutating diode in a motor control circuit. In this case, if the reverse voltage is charged immediately after a high current is supplied to the diode, it may be destroyed depending on the circuit and the operating conditions.

Fig. 4-63 and 4-64 shows a basic motor control circuit and the waveform of the motor control operation. These waveforms are at Q_2 and Q_3 off and Q_1 and Q_4 on. Q_4 is continuously on when Q_1 is chopping.

At gate drive signal entering G_1, Q_1 turns on and i_{D1} flows. When the current i_{D1} of Q_1 stops, the regenerative current i_F flows through the built-in diode of Q_2, by energy stored in the inductance of the motor. In this state, if Q_1 turns on, Q_2 is shortened because of the reverse recovery time t_{rr} of the built-in diode of Q_2, and excess recovery current i_{Dr} flows.

This excess recovery current may destroy the diode at a point in the shaded area in the figure, which indicates the period in which the built-in diode voltage recovers. Therefore, restricting the recovery current i_{Dr} is an effective method to prevent diode destruction. Table 4-6 shows the detailed circuit countermeasures.

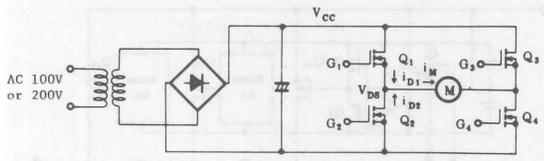
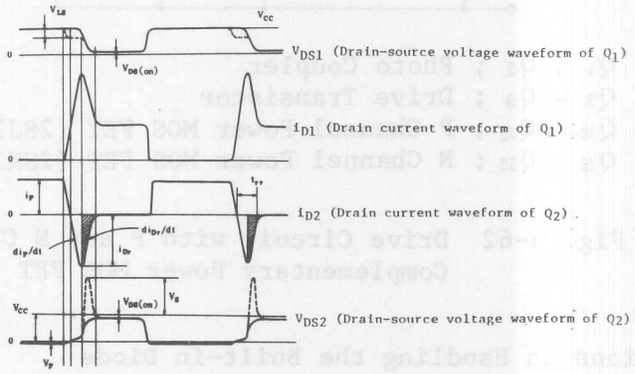


Fig. 4-63 Basic Motor Control Circuit

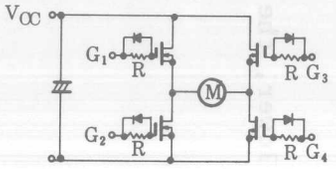
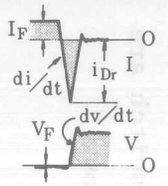
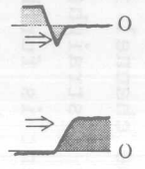
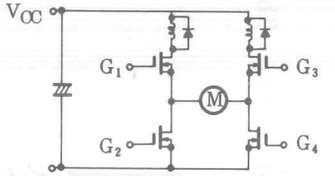
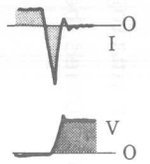
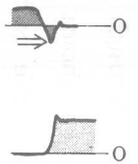
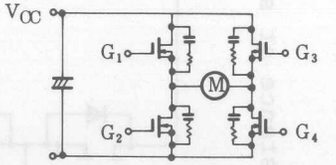
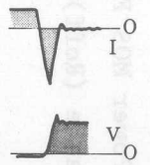
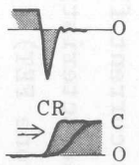
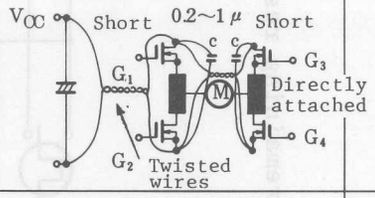
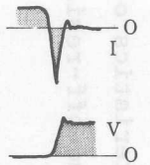
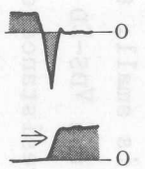
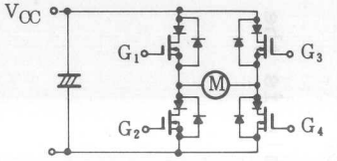
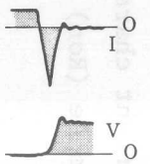
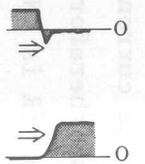


<Description>

i_F : Forward current of Q_2 built-in diode
V_F : Forward voltage drop of Q_2 built-in diode
$V_{DS(on)}$: Drain-source saturation voltage of Q_2
t_{rr}: Reverse recovery time of Q_2 built-in diode
V_{LS}: Voltage drop with circuit inductance Ls
i_{Dr}: Reverse recovery current of Q_2 built-in diode
(depends on the drive signal source impedence di_F/dt of Q_1, circuit inductance Ls, supply voltage V_{CC}, and electric charge Q_{rr} (or t_{rr}) in the built-in diode)
V_S : Spike voltage
(depends on the inductance Ls, i_{DR}, and di_{DR}/dt of the circuit)

Fig. 4-64 Waveform of the Motor Control Operation

Table 4-6 Circuit Countermeasures against Built-in Diode Destruction

Classification	Countermeasures	Circuit	Waveforms of the built-in diode		Circuit constants, etc.
			Before improvement	After improvement	
①	Delay the turn-on time, by inserting a resistor and diode which are connected in parallel into the gate of the Power MOS FET. This controls di/dt and dv/dt of the built-in diode to restrict the recovery current (in this case, the turn-off time does not have to be delayed).				R = 330Ω ~ 820Ω (di/dt = 20 ~ 50A/μs)
②	Insert an L and diode connected in parallel into the drain of the Power MOS FET. This controls di/dt to restrict the recovery current i_{Dr}.				L = 2 μH ~ 20 μH
③	Insert a C or CR snubber between the drain and source of the Power MOS FET to restrict dv/dt and voltage spike of the built-in diode.				R = 10 ~ 47Ω C = 0.01 μF ~ 0.1 μF Wiring of the snubber should be as short as possible.
④	Wires between + , - terminals of the power supply line and the drain/source of each arm (in the case of N/N) should be twisted C are also connected. By directly attaching wires to the upper and lower arms and minimizing stray the inductance, the voltage spike and dv/dt are restricted.				Should be done together with countermeasures ① to ③.
⑤	Connect the fast diode to the external of the Power MOS FET not to flow the current in the built-in diode.				

4.5 Analog Switch

When two power MOS FET's are connected in series, they operate as a two-way analog switch (Fig. 4-65).

Remember that the power MOS FET is made to have a diode between drain and source. When applying a positive bias between gate and source, the V_{DS} vs. I_D characteristics are as shown in Fig. 4-66.

When the current is small, the current flows through the channel in both FET's, therefore the V_{DS}-I_D characteristics is shown by a straight line of 2×R (R is ON resistance of one FET). When the current is further increased, it will flow through the diode of one FET and the V_{DS}-I_D characteristics approaches the diode characteristics.

Important characteristics of Power MOS FET for analog switch are on-resistance (Ron) and off-resistance (Roff) mentioned below.

(1) Ron

This is the remaining resistance at switch on. The lower, the better.

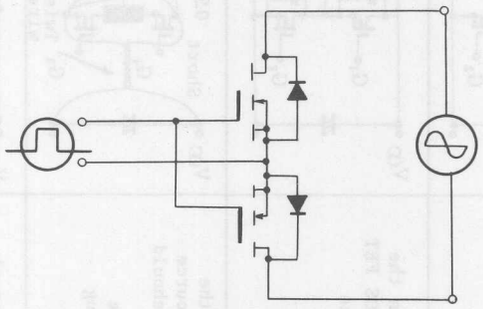


Fig. 4-65 Analog Switch

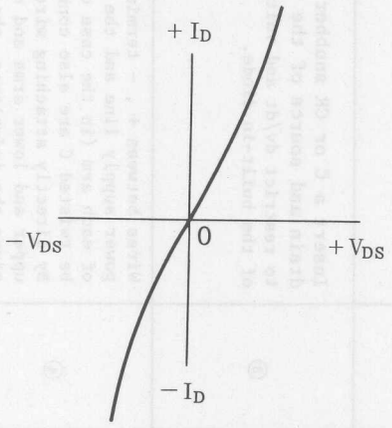


Fig. 4-66 V_{DS}-I_D Characteristics

(2) R_{off}

R_{off} is the resistance between the ends of the switch when the switch is open and is equivalent to insulation resistance of mechanical switch. The higher this resistance is, the better the switch is. It means that leak current (I_{DSS}, I_{DSX}) is small. (Several nA to several ten nA in general)

In low current area, R_{on} of the built-in diode of Power MOS FET can be small, applying positive gate-source bias (Fig. 4-67). It is superior to diode switch. When the gate-source bias is 0 or negative, the characteristics are the same as that of general diode. As Power MOS FET has enhancement characteristics, leak current remains unchanged when V_{GS} is applied 0.5 ~ 1.0V positive bias induced by, such as, external circuit noise.

Power MOS FET can show its ability to a bi-directional (it can switch alternative current) analog switch which has good linearity.

The characteristics of 2SK294 is shown in Fig. 4-68.

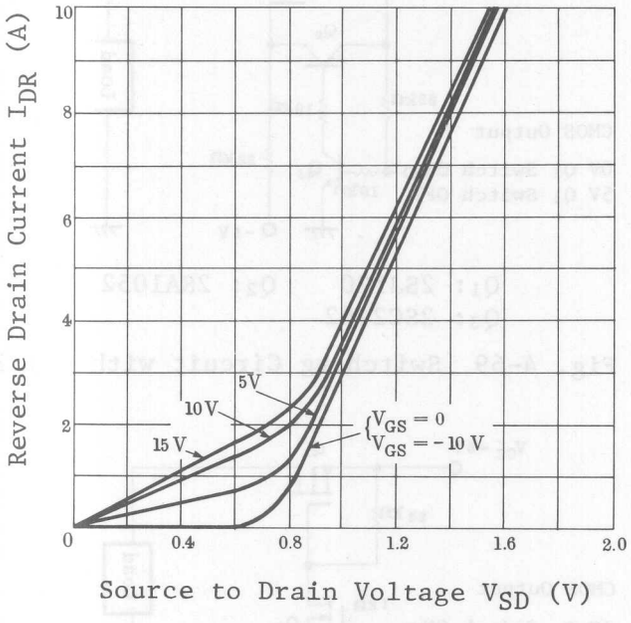


Fig. 4-67 Characteristics of Built-in Diode (2SK294)

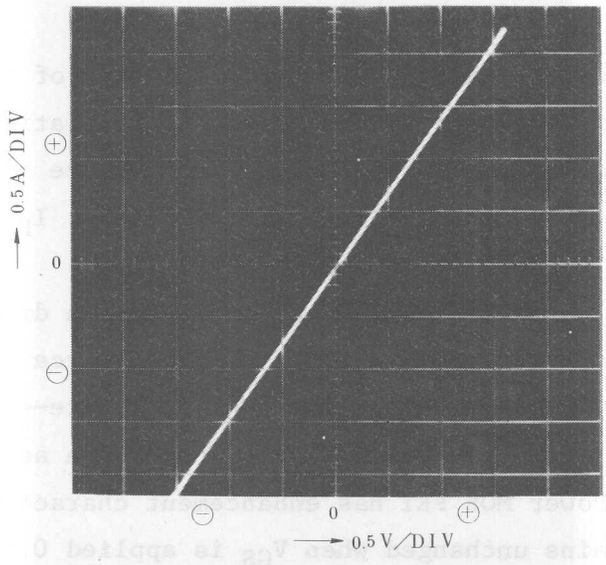
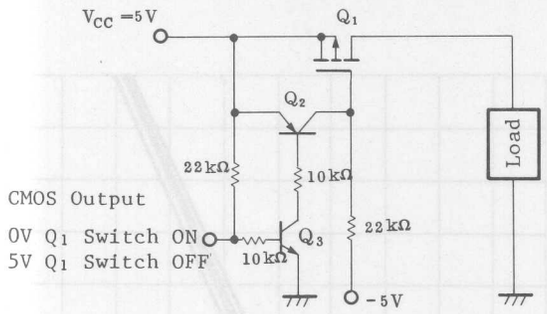


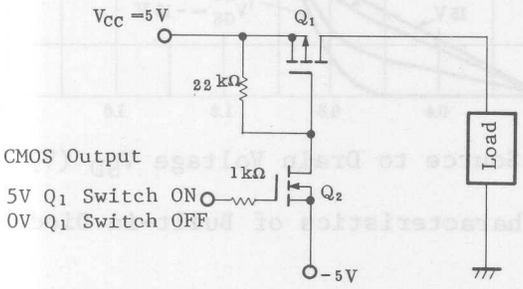
Fig. 4-68 Characteristics of 2SK294

The switching circuits, in which 2SJ120 and 2SJ121 are used, are shown in Fig. 4-69 and 4-70.



Q_1: 2SJ120 Q_2: 2SA1052
Q_3: 2SC2462

Fig. 4-69 Switching Circuit with 2SJ120



Q_1: 2SJ121
Q_2: 2SK416

Fig. 4-70 Switching Circuit with 2SJ121

4.6 Character Display

The recent increase in office automation has lead to the need for higher resolution color and monochrome displays requiring bandwidths of 40 to 80 MHz. To meet these requirements, the transistor used for video output should have high breakdown voltage, small I/O capacitances and excellent high frequency characteristics.

In a transistor, the breakdown voltage and the high frequency characteristics are contrary to each other, so it is difficult to realize 40 to 80MHz bandwidth current bipolar transistors for video output, because of their high frequency characteristics. By using the 2SK352 in high-resolution cathode-ray tube displays this bandwidth can be realized.

4.6.1 Features

Since the 2SK511 is designed to have small I/O capacitance and high gm, it can be used not only for video output but also for high-output, wide-band, high-impedance amplifiers in measuring instruments, etc. Table 4-7 and Table 4-8 show the absolute maximum ratings and the electrical characteristics respectively.

Table 4-7 ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	250	V
Gate to Source Voltage	V_{GSS}	±9	V
Drain Current	I_D	0.3	A
Drain peak Current	I_D(peak)	0.5	A
Channel Dissipation	Pch*	8	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55∿+150	°C

*T_C=25°C

Table 4-8 ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA , V_{GS}=0	250	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±9V , V_{DS}=0	-	-	± 1	mA
Drain Current	I_{DSS}	V_{DS}=200V , V_{GS}=0	-	-	1	mA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=0.1A , V_{GS}=9 V	-	3.0	5.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=0.15A , V_{DS}=20V	50	80	-	mS
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	20	-	pF
Output Capacitance	Coss		-	10	-	pF
Reverse Transfer Capacitance	Crss		-	2.5	-	pF

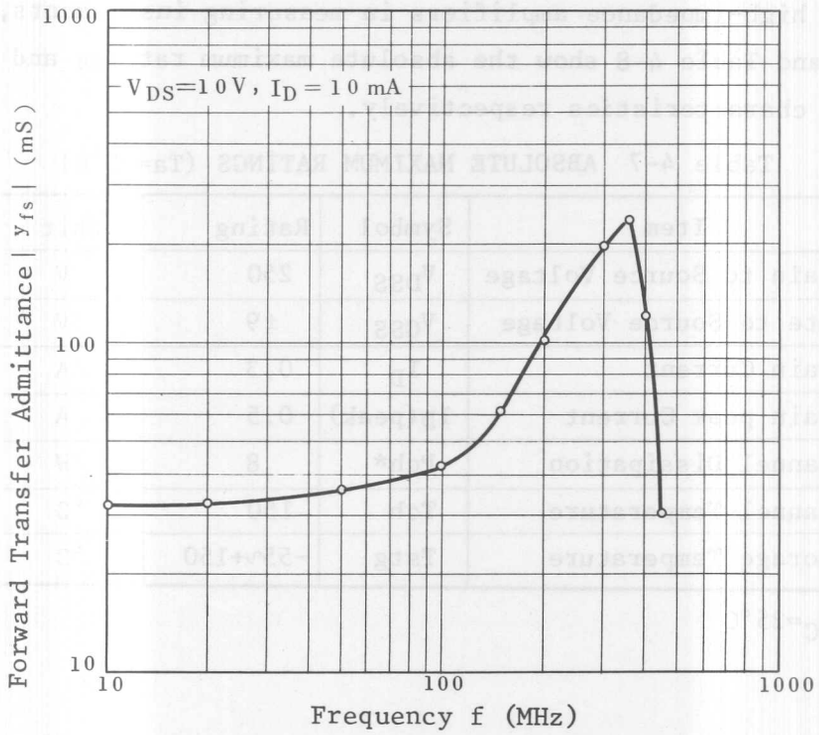


Fig. 4.71 $|y_{fs}|$ -f Characteristics

● Excellent high frequency characteristics

The 2SK511 has high cut-off frequency (f_C), 250MHz (typ). Compared with that of bipolar transistors (f_T=80MHz(typ); i.e. f_C=5MHz), it is 50 times higher. Fig. 4-71 shows $|y_{fs}|$ vs. frequency characteristics.

● Small I/O capacitances

In video amplifiers, the band width depends on the output capacitance (Coss). In the 2SK511, the output capacitance (Coss) is reduced to 10pF, and the input capacitance (Ciss), 20pF.

With small I/O capacitances, a high amplification factor is obtained, without reducing the mutual conductance($|y_{fs}|$ =80mS(typ)).

● ASO(Area of Safe Operation)

The 2SK511 has no secondary breakdown area. The rating of Pch=8W is guaranteed to the extent of V_{DS}=250V.

4.6.2 Application Notes

We would like to describe the use of the 2SK511 in a video output stage.

● Wide Band Width

The I/O capacitances of the 2SK511 are small, and to further reduce their effect, the common gate connection is recommended. In this case, the source will be driven by high speed TTL or a high speed switching transistor (2SC3652 etc.)

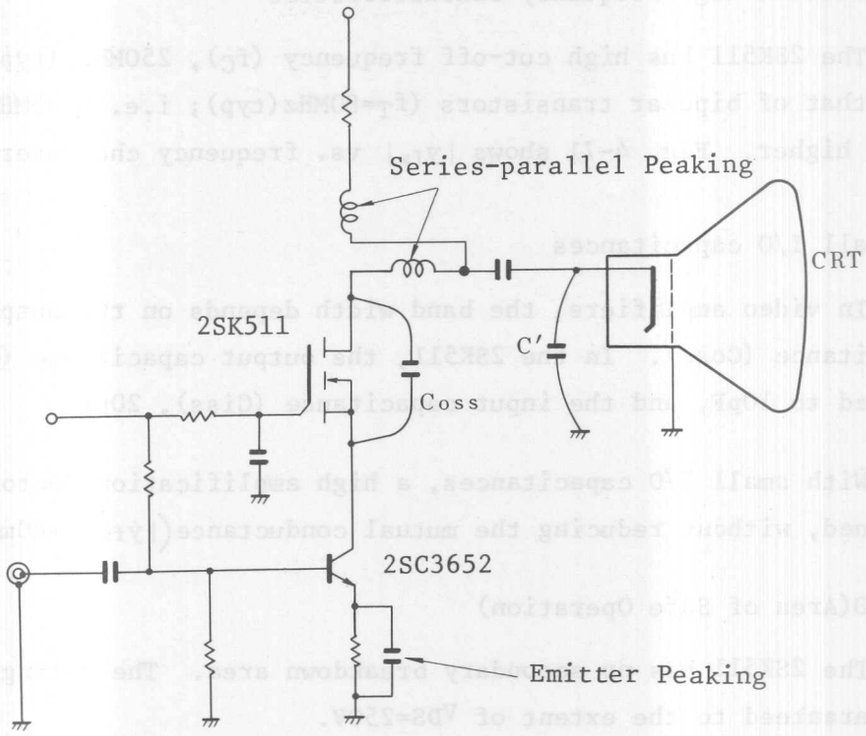


Fig. 4-72 Video Output Circuit

Generally, the high cut-off frequency of a RC coupled amplifier is determined by load resistance (R_L), the output capacitance (Coss) of the transistor and the cathode-ray tube's capacitance (C'). Therefore, to take advantage of the high frequency characteristics of the 2SK511, we recommend use of parallel, series, and emitter peaking. When using the 2SK352 in the digital (switching) mode, use a speed-up capacitor.

The 2SC3025 and the 2SC3026 (V_{CBO}=1500V, 1700V, I_C=5A, fall time t_f=0.5μs max.) are horizontal deflection output transistors for television receivers.

4.7 Ultrasonic Equipment

We would like to describe the power MOS FETs use in ultrasonic wave diagnostic equipment. Formerly, bipolar transistors have been used for high-voltage and high-speed switching devices used to generate pulse voltage for ultrasonic wave diagnostic equipment. Recently, as ultrasonic wave diagnostic equipment is required to have higher performance and higher operating frequency, the power MOS FETs small package, high breakdown voltage, and low ON resistance has LED to its use.

Fig. 4-73 shows the block diagram and Fig. 6-54 shows the high voltage pulse generator circuit and the voltage waveform. This circuit has the following functions. 1) The pulse voltage (V_{p-p}) is as large as possible 2) The frequency component of the pulse voltage oscillation waveform is high. The power MOS FET provides high switching speed and excellent frequency characteristics. By using power MOS FETs, ultrasonic wave diagnostic equipment can operate with high frequency and meets the conditions (1) and (2), resulting in clear pictures.

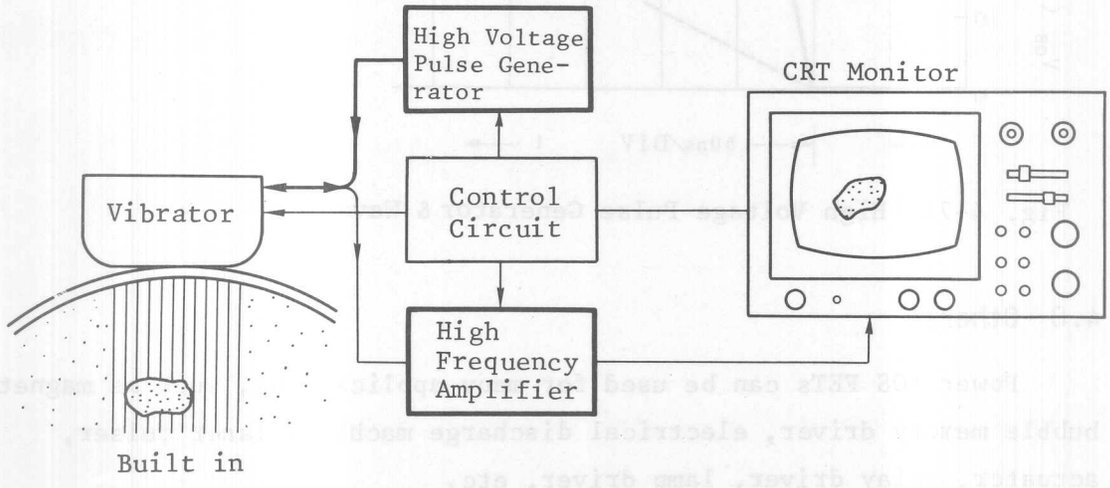


Fig. 4-73 Block Diagram

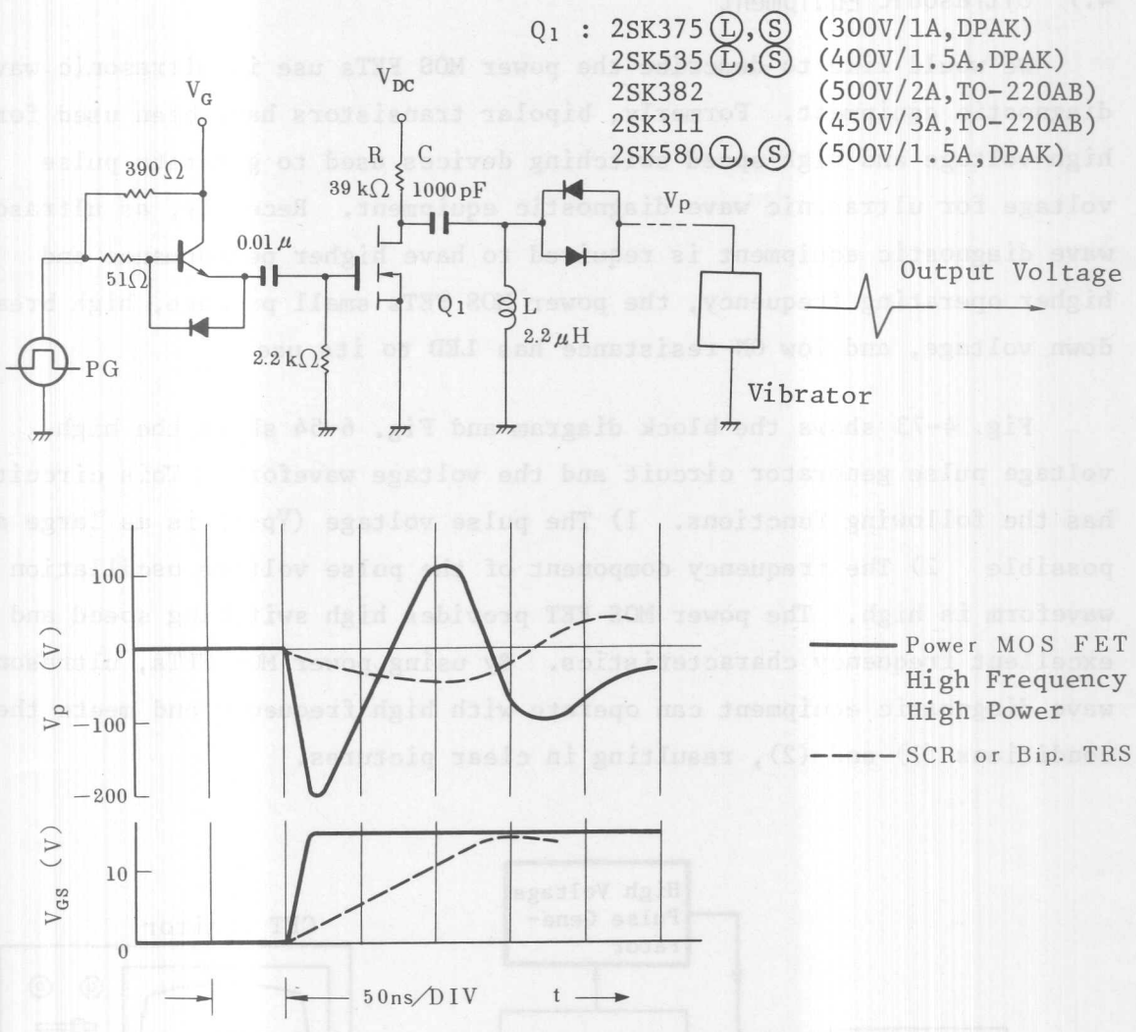


Fig. 4-74 High Voltage Pulse Generator & Waveform

4.8 Others

Power MOS FETs can be used for many applications, such as magnetic bubble memory driver, electrical discharge machine, laser pulser, actuator, relay driver, lamp driver, etc.

Reference Books

*1) Kurisu, Yoshida, Kiyama, Full---transistorized Medium Wave Broadcasting Transmitter Using Power MOS FET

*2) Aoyagi, Inoue, "Short Wave Broadcasting Transmitter using FET", Television Academy Technology Report, RE79-24